

Compal Confidential

Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

Compal Confidential

P7YE0/P7YH0/P7YS0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
ATI Seymour/Whistler/Granville

2010-11-01

REV:0.3

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address	VRAM P/N	
ChannelA	DIMM0 A0 1010 000X JDIMM1	SAM 64*16 900M SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABOI)	
	DIMM1 A2 1010 001X JDIMM3	SAM 64*16 800M SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABOI)	
		SAM 128*16 800M SA00003MG60(S IC D3 128M16 K4W2G1646C-HC12 FBGA ABOI)	
ChannelB	DIMM0 A4 1010 010X JDIMM2	HYN 64*16 900M SA000041SA0(S IC D3 64MX16 H5TQ1G63DPR-11C FBGA ABOI)	
	DIMM1 A6 1010 011X JDIMM4	HYN 64*16 800M SA000032420(S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABOI)	
		HYN 128*16 800M SA00003VS10(S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABOI)	
		HYN 64*16 800M SA0000324G0(S IC D3 64M16 H5TQ1G63DPR-12C FBGA ABOI)	
BT Config GPU config BACO config			
BT SKU:	BT@ Whistler: WHIS@	BACO:	BACO@
4DIMM config	Seymour: SEYM@	nonBACO:	NOBACO@
4 DIMM:	4DIMM@ Granville: GRAN@	Muxless config	
LVDS/eDP config	Granville config	Muxless:	MUXL@
UMA LVDS:	ULVDS@ Granville: GRAN@ (VDDCI)	nonMuxless:	NOMUXL@ (DISO,UMAO)
DIS LVDS:	DLVDS@ nonGranville: NOGRAN@ (VGA_CORE)		
DIS eDP:	DEDP@ GPU Frame config		
	128bit: 128@ (WHIS,GRAN)		
VRAM BOM Config			
	X76264BOL01: 64Mx16x4 Seymour	512M HYN NEW	
	X76264BOL02: 64Mx16x4 Seymour	512M HYN OLD	
	X76264BOL03: 64Mx16x8 Whistler/Granville	1G HYN NEW	
	X76264BOL04: 64Mx16x8 Whistler/Granville	1G HYN OLD	
	X76264BOL05: 128Mx16x8 Whistler/Granville	2G HYN	
	X76264BOL06: 128Mx16x8 Whistler/Granville	2G SAM	
	X76264BOL07: 128Mx16x4 Seymour	1G SAM	
	X76264BOL08: 128Mx16x4 Seymour	1G HYN	
BOM Config			
* UMA Only LVDS Panel:	BT@UMAO@/UMA@/ULVDS@/NOMUXL@	+DIMM,USB option	
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+X76+GPU	+DIMM,USB option
DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+X76+GPU	+DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+X76+GPU(S,W)	+DIMM,USB option
Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@	+X76+GPU(G)	+DIMM,USB option

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
		2	USB port(left side 2.0)
	UHCI1	3	USB/B(Right side 3.0 option)
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card(WLAN)
	UHCI4	9	Mini Card
		10	Camera
	UHCI5	11	Card Reader
		12	
		13	Blue Tooth
	UHCI6		

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Muxless/UMA	UMA@
DIS Only	DISO@
Muxless/DIS	DIS@
Muxless/DIS	VGA@
BACO mode	BACO@
nonBACO mode	NOBACO@
VRAM	X76@
128bit VRAM	128@
Granville GPU	GRAN@
Whistler GPU	WHIS@
Seymour GPU	SEYM@
non Granville GPU	NOGRAN@
Blue Tooth	BT@
Connector	CONN@
Unpop	@
DIS eDP	DEDP@
UMA LVDS	ULVDS@
DIS LVDS	DLVDS@
Muxless	MUXL@
non Muxless	NOMUXL@
USB2.0 Conn	USB2@
USB3.0 Conn	USB3@
4 Dimm	4DIMM@

P9,P19,P23,P30-32,P59  
P4,P14  
P.22-28  
P.26 ,P.29  
P.27,28  
P.27  
P.23,P.59  
P.59  
P.22-26  
P.23,P.25  
P.35

P.30,59  
P.30  
P.18,P.32  
P.41  
P.41  
P.11-12

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG\_GTX\_HRX\_N[0..15] 22  
PEG\_GTX\_HRX\_P[0..15] 22  
PEG\_HTX\_C\_GRX\_N[0..15] 22  
PEG\_HTX\_C\_GRX\_P[0..15] 22

15 DMI\_CRX\_PTX\_N0  
15 DMI\_CRX\_PTX\_N1  
15 DMI\_CRX\_PTX\_N2  
15 DMI\_CRX\_PTX\_N3  
15 DMI\_CRX\_PTX\_P0  
15 DMI\_CRX\_PTX\_P1  
15 DMI\_CRX\_PTX\_P2  
15 DMI\_CRX\_PTX\_P3  
15 DMI\_CTX\_PTX\_N0  
15 DMI\_CTX\_PTX\_N1  
15 DMI\_CTX\_PTX\_N2  
15 DMI\_CTX\_PTX\_N3  
15 DMI\_CTX\_PTX\_P0  
15 DMI\_CTX\_PTX\_P1  
15 DMI\_CTX\_PTX\_P2  
15 DMI\_CTX\_PTX\_P3

15 FDI\_CTX\_PTX\_N0  
15 FDI\_CTX\_PTX\_N1  
15 FDI\_CTX\_PTX\_N2  
15 FDI\_CTX\_PTX\_N3  
15 FDI\_CTX\_PTX\_N4  
15 FDI\_CTX\_PTX\_N5  
15 FDI\_CTX\_PTX\_N6  
15 FDI\_CTX\_PTX\_N7  
15 FDI\_CTX\_PTX\_P0  
15 FDI\_CTX\_PTX\_P1  
15 FDI\_CTX\_PTX\_P2  
15 FDI\_CTX\_PTX\_P3  
15 FDI\_CTX\_PTX\_P4  
15 FDI\_CTX\_PTX\_P5  
15 FDI\_CTX\_PTX\_P6  
15 FDI\_CTX\_PTX\_P7

15 FDI\_FSYNCO  
15 FDI\_FSYNC1  
15 FDI\_INT  
15 FDI\_LSYNCO  
15 FDI\_LSYNC1

15 FDI\_FSYNCO  
15 FDI\_FSYNC1  
15 FDI\_INT  
15 FDI\_LSYNCO  
15 FDI\_LSYNC1

15 FDI\_FSYNCO  
15 FDI\_FSYNC1  
15 FDI\_INT  
15 FDI\_LSYNCO  
15 FDI\_LSYNC1

JCPU1A

DMI

FDI

Intel(R) FDI

eDP

PCI EXPRESS\* - GRAPHICS

PEG\_ICOMPI  
PEG\_ICOMPO  
PEG\_RCOMPO

PEG\_RX#0  
PEG\_RX#1  
PEG\_RX#2  
PEG\_RX#3  
PEG\_RX#4  
PEG\_RX#5  
PEG\_RX#6  
PEG\_RX#7  
PEG\_RX#8  
PEG\_RX#9  
PEG\_RX#10  
PEG\_RX#11  
PEG\_RX#12  
PEG\_RX#13  
PEG\_RX#14  
PEG\_RX#15

PEG\_RX#0  
PEG\_RX#1  
PEG\_RX#2  
PEG\_RX#3  
PEG\_RX#4  
PEG\_RX#5  
PEG\_RX#6  
PEG\_RX#7  
PEG\_RX#8  
PEG\_RX#9  
PEG\_RX#10  
PEG\_RX#11  
PEG\_RX#12  
PEG\_RX#13  
PEG\_RX#14  
PEG\_RX#15

PEG\_TX#0  
PEG\_TX#1  
PEG\_TX#2  
PEG\_TX#3  
PEG\_TX#4  
PEG\_TX#5  
PEG\_TX#6  
PEG\_TX#7  
PEG\_TX#8  
PEG\_TX#9  
PEG\_TX#10  
PEG\_TX#11  
PEG\_TX#12  
PEG\_TX#13  
PEG\_TX#14  
PEG\_TX#15

PEG\_TX#0  
PEG\_TX#1  
PEG\_TX#2  
PEG\_TX#3  
PEG\_TX#4  
PEG\_TX#5  
PEG\_TX#6  
PEG\_TX#7  
PEG\_TX#8  
PEG\_TX#9  
PEG\_TX#10  
PEG\_TX#11  
PEG\_TX#12  
PEG\_TX#13  
PEG\_TX#14  
PEG\_TX#15

Sandy Bridge\_rPGA\_Rev0p61  
CONN@

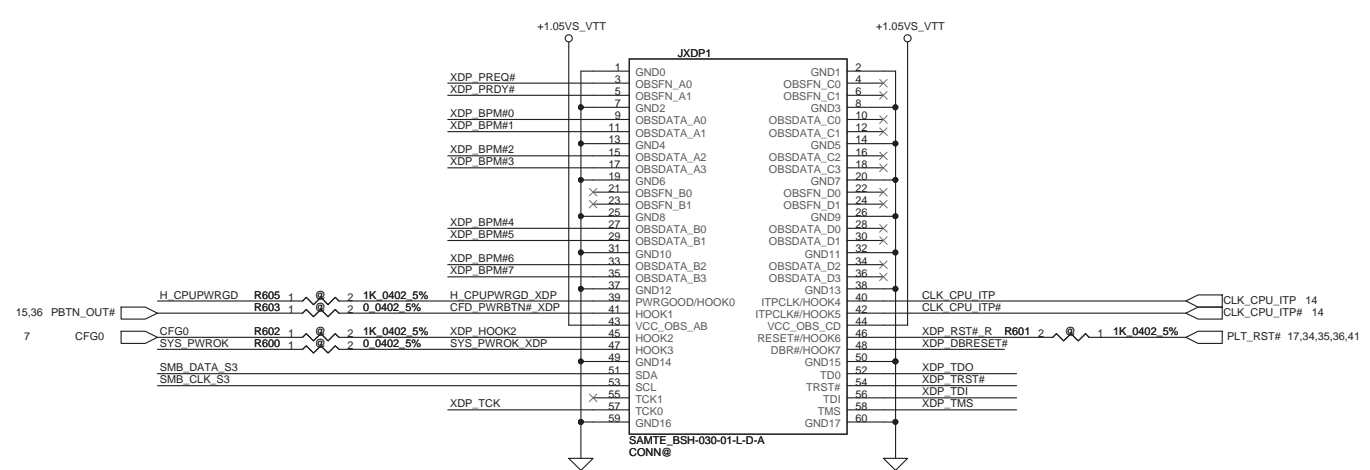
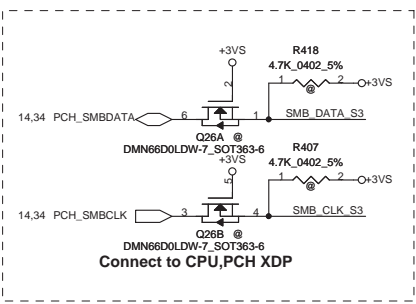
+1.05VS\_VTT  
R532  
24.9\_0402\_1%

+1.05VS\_VTT  
R118  
24.9\_0402\_1%

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms should not be left floating ,even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

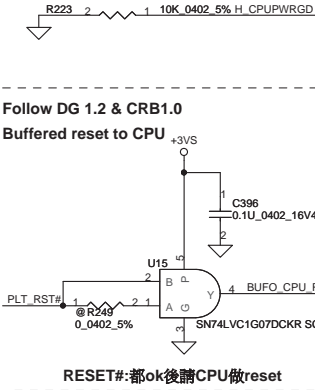
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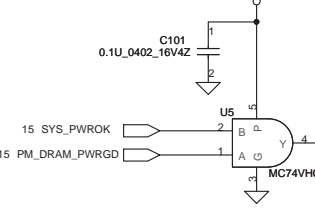
Debug port DG 0.65-  
Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed

PCH->CPU  
UNCOREPWRGOOD:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok  
RESET#:都ok後請CPU做reset

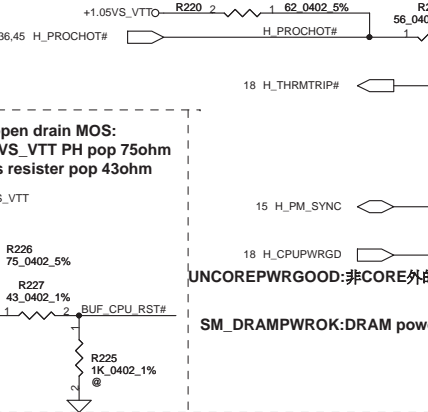
Follow DG 1.2 & CRB1.0



Follow DG 1.2 & CRB1.0



Processor Pullups follow CRB1.0



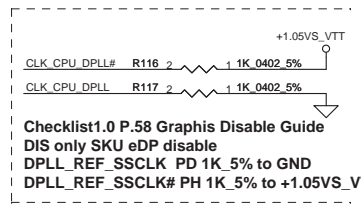
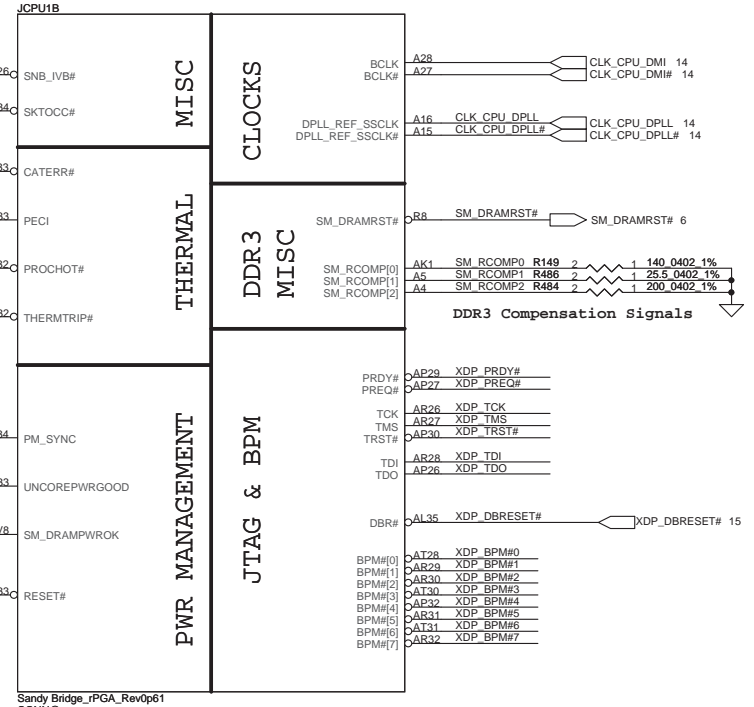
UNCOREPWRGOOD:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok

Use open drain MOS:  
+1.5V\_CPU\_VDDQ PH pop 200ohm  
series resistor pop 130ohm

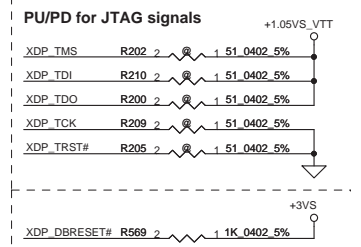
PROC\_SELECT#  
Future platforms,PH VCPLL and connect to PCH DF\_TV5

偵測CPU有無安裝

XBOX三紅功能

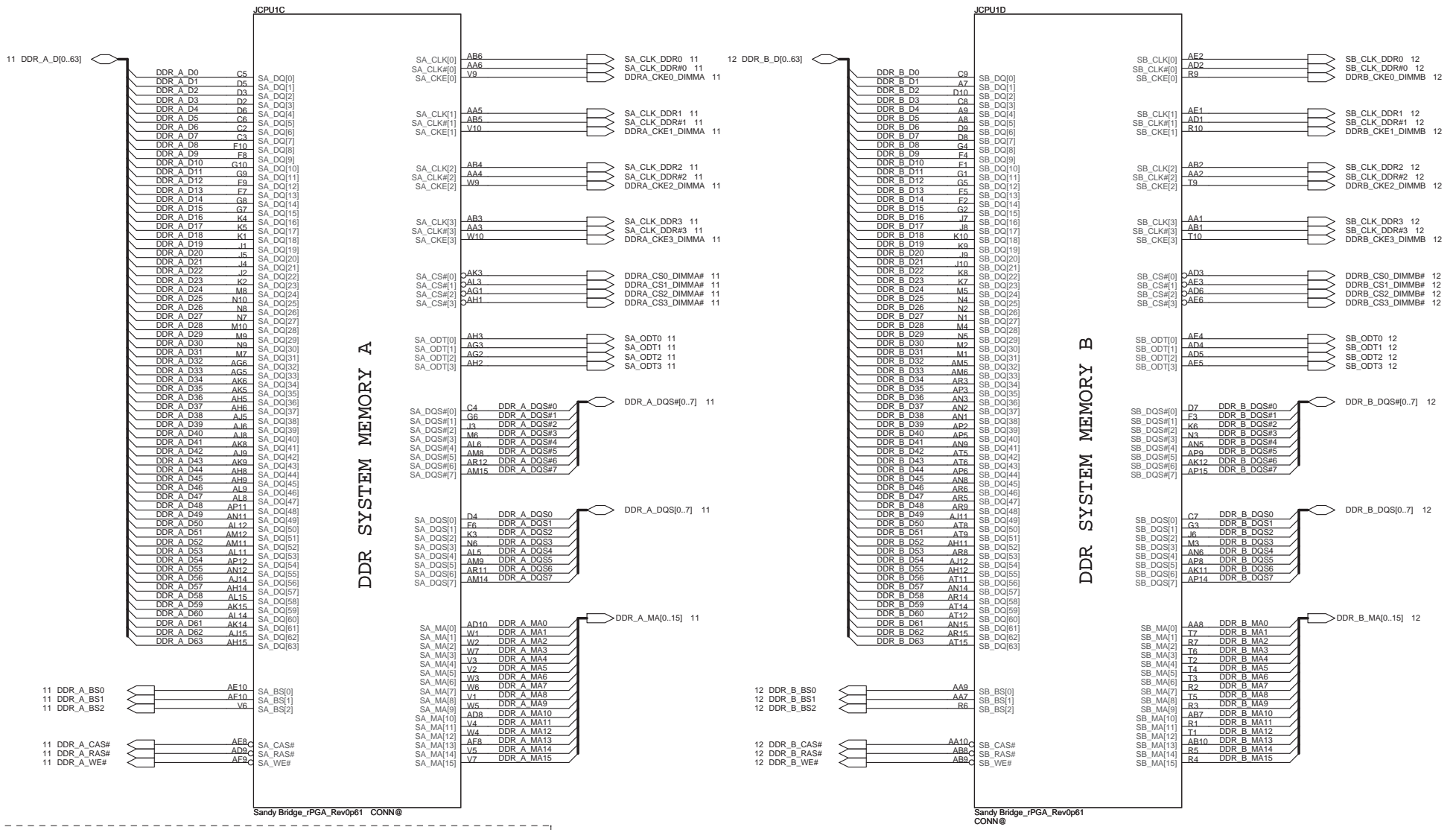


Checklist.1.0 P.58 Graphis Disable Guide  
DIS only SKU eDP disable  
DPLL\_REF\_SSCLK PD 1K\_5% to GND  
DPLL\_REF\_SSCLK# PH 1K\_5% to +1.05VS\_VTT



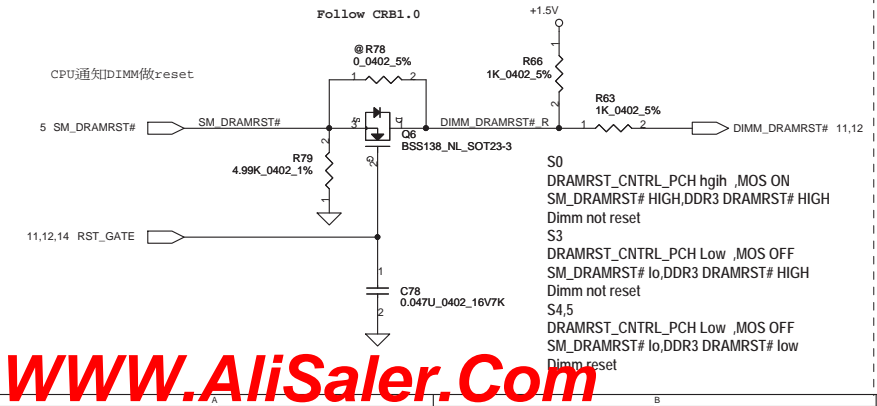
CRB1.0 PH 1K +3VS  
Check list 1.0 PH 5K +3VS  
Check list 1.2 PH 10K +3VS  
Debug port DG1.1-1.2 50-5K ohm

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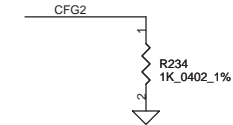


S0  
DRAMRST#\_CNTRL\_PCH high, MOS ON  
SM\_DRAMRST# HIGH, DDR3 DRAMRST# HIGH  
Dimm not reset  
S3  
DRAMRST#\_CNTRL\_PCH Low, MOS OFF  
SM\_DRAMRST# Lo, DDR3 DRAMRST# HIGH  
Dimm not reset  
S4,5  
DRAMRST#\_CNTRL\_PCH Low, MOS OFF  
SM\_DRAMRST# Lo, DDR3 DRAMRST# low  
Dimm reset

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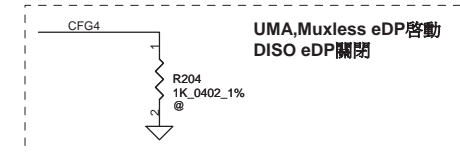


## CFG Straps for Processor



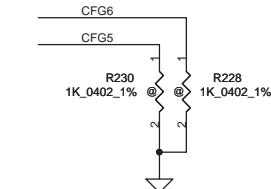
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	------------------------------------------------------------------------------------------------



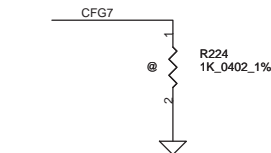
eDP enable

CFG4	★ 1: Disable 0: Enable
------	---------------------------



PCIe Port Bifurcation Straps

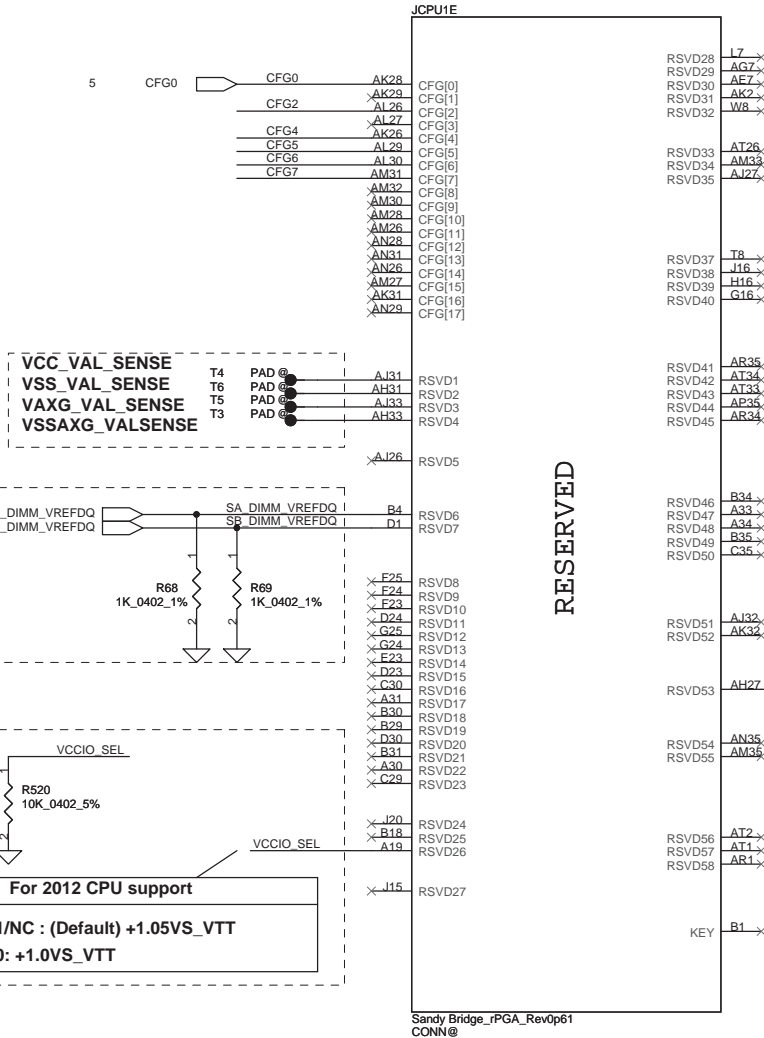
CFG[6:5]	★11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express
----------	---------------------------------------------------------------------------------------------------



PEG DEFER TRAINING

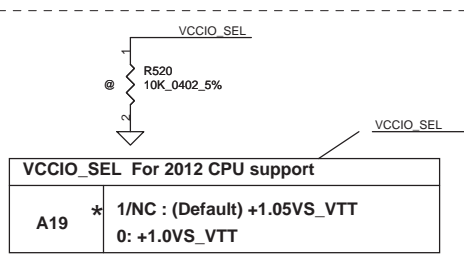
CRB1.0 P.12

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---------------------------------------------------------------------------------------------------------



Sandy Bridge\_rPGA\_Rev0p61  
CONN@

SA\_DIMM\_VREFDQ  
SB\_DIMM\_VREFDQ  
For Future CPU M3 support,  
Sandy bridge not support M3,  
Check list1.0&CRB say can NC



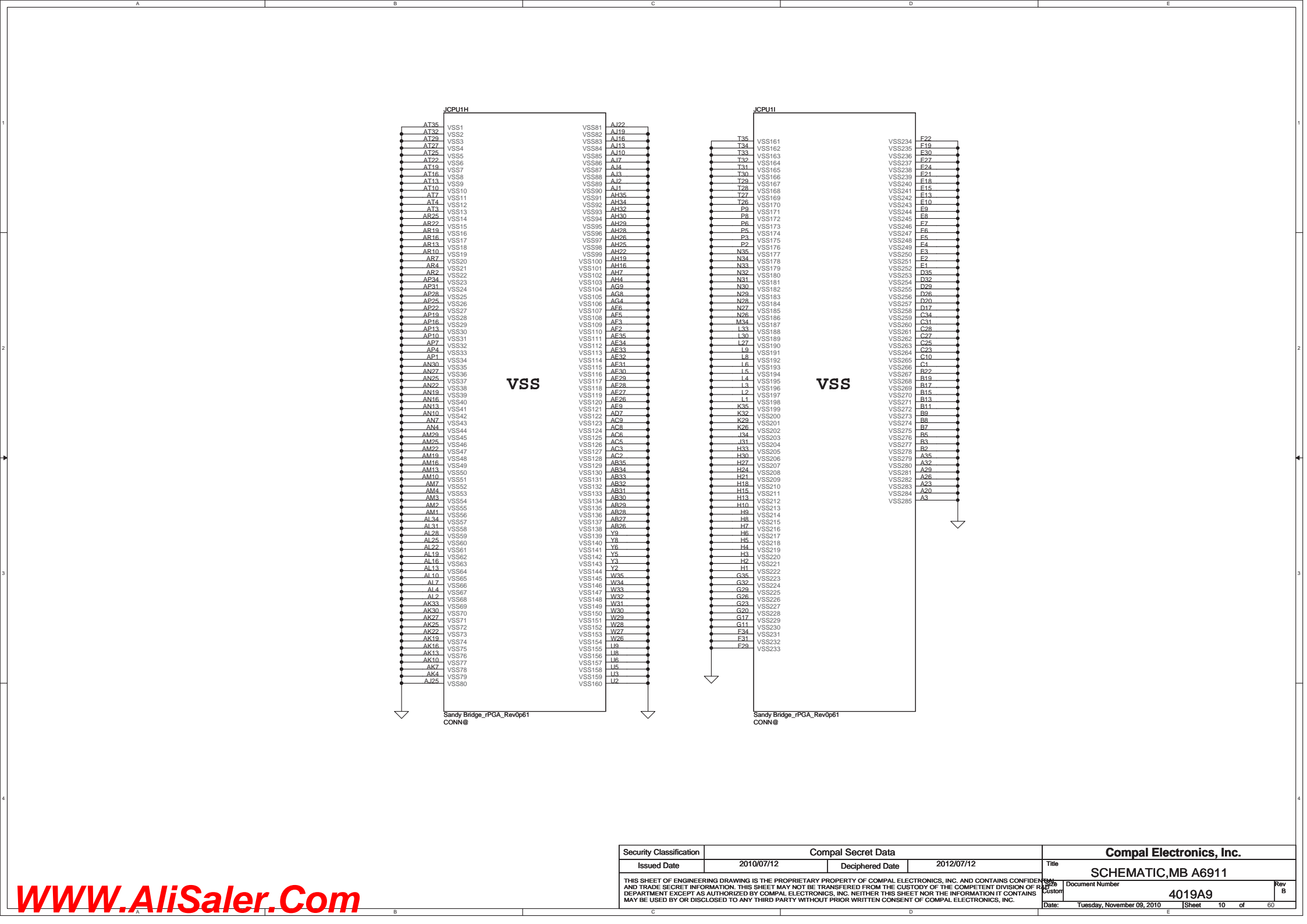
A19	★ 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT
-----	-------------------------------------------------

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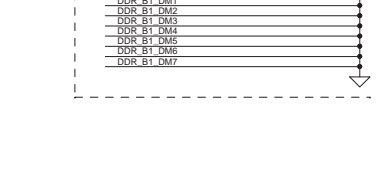
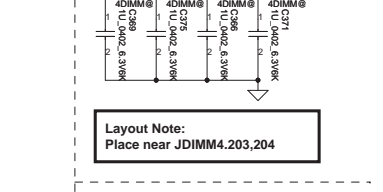
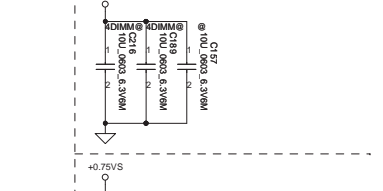
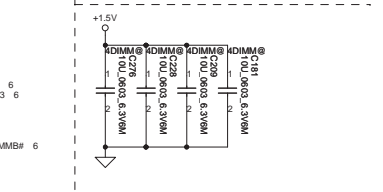
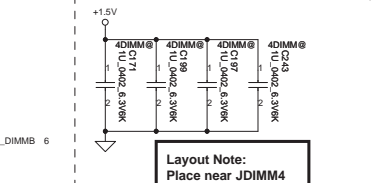






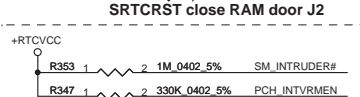
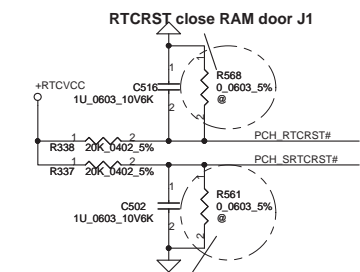






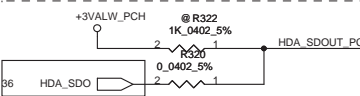
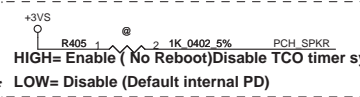
### Channel B

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			Date Issued 12/09/2010 Date Issued 12/09/2010	Date Issued 12/09/2010 Date Issued 12/09/2010	



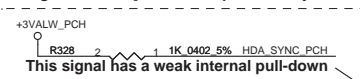
**INTVRMEN**

\* H : Integrated VRM enable  
L : Integrated VRM disable  
(INTVRMEN should always be pull high.)



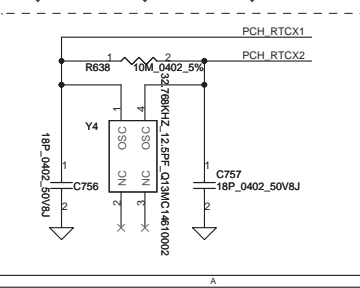
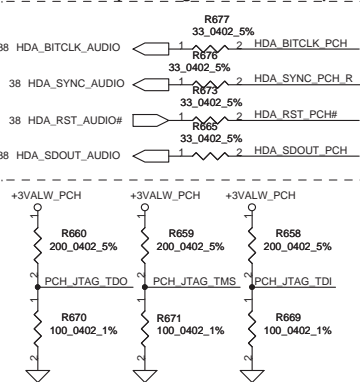
**ME debug mode this signal has a weak internal PD**

\* Low = Disabled (Default)  
High = Enabled (Flash Descriptor Security Override)

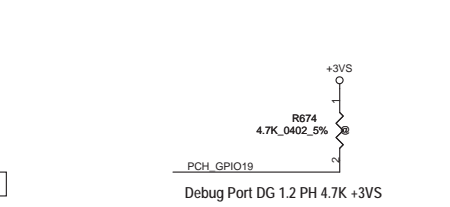
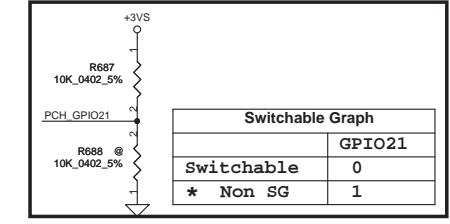
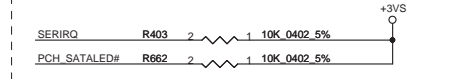
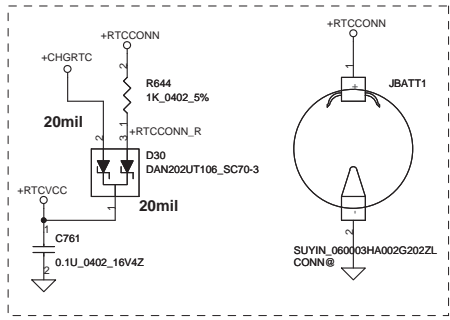
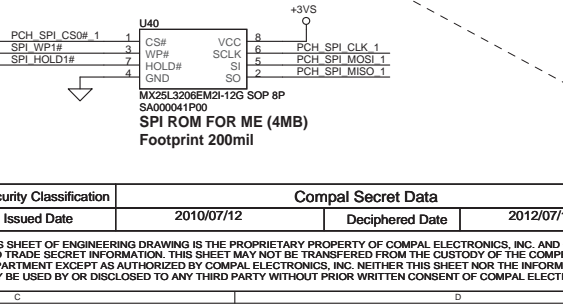
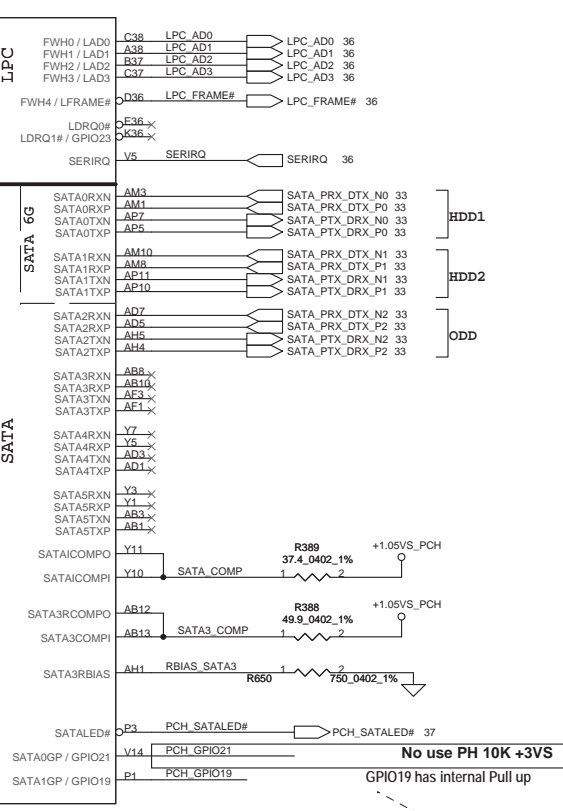
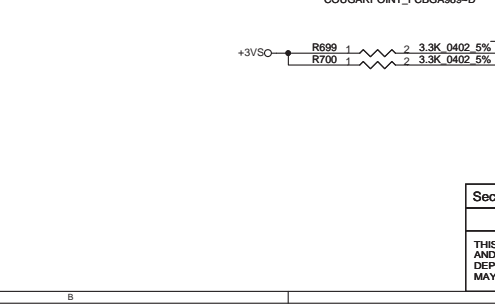
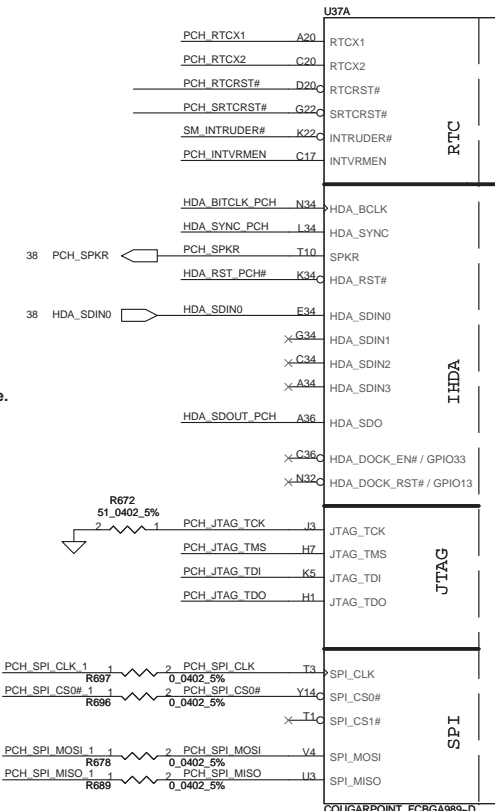
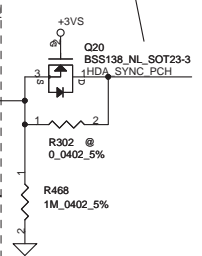


**On Die PLL VR Select is supplied by**

\*1.5V when sampled high  
1.8V when sampled low  
Needs to be pulled High for Huron River platform



Prevent back drive issue.

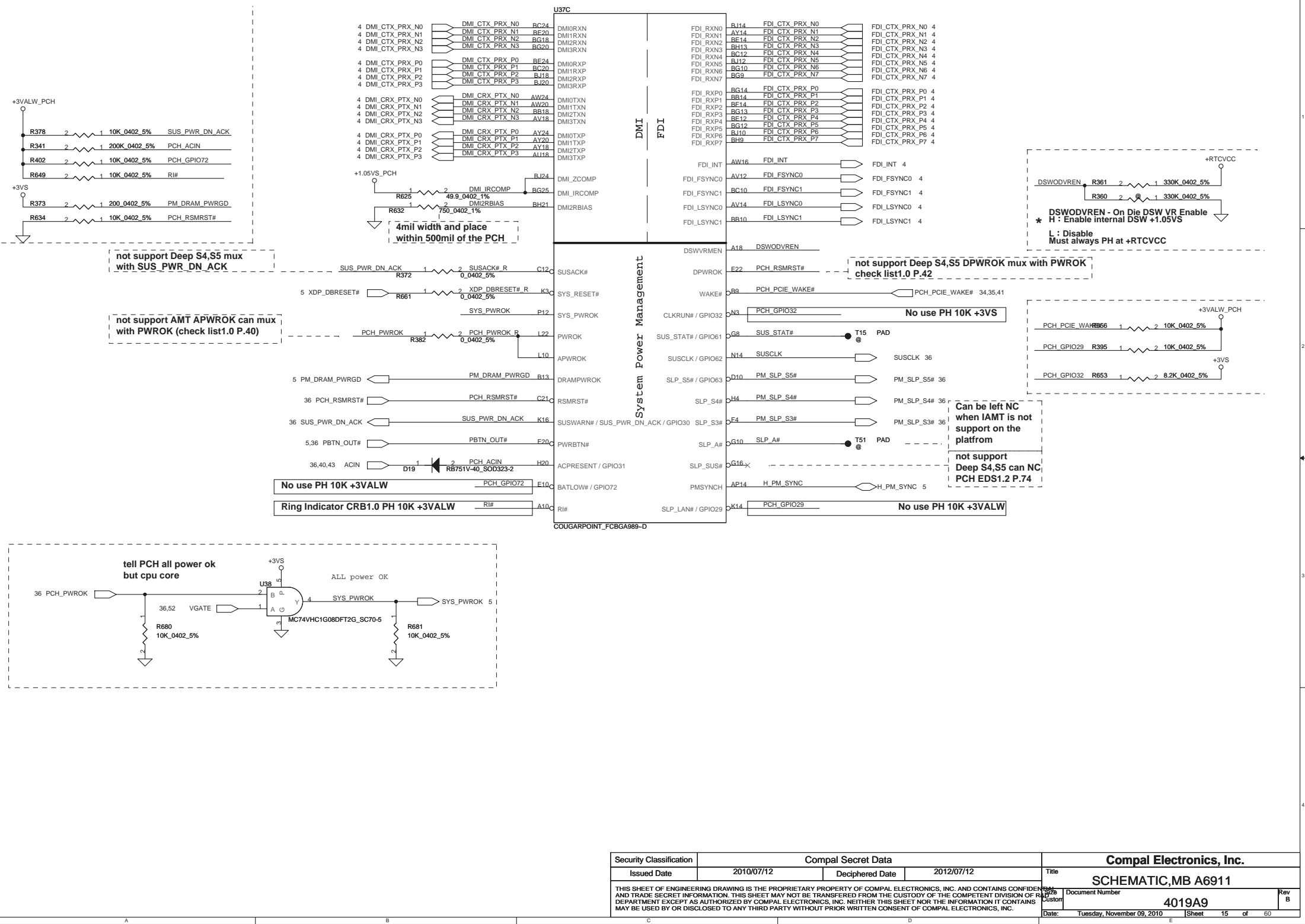


Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

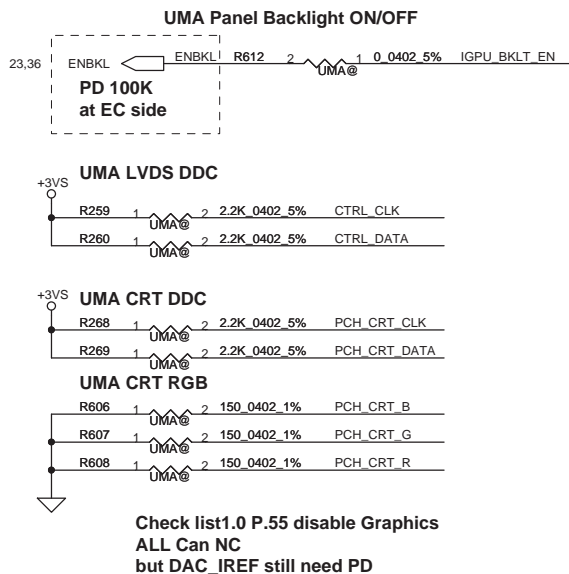








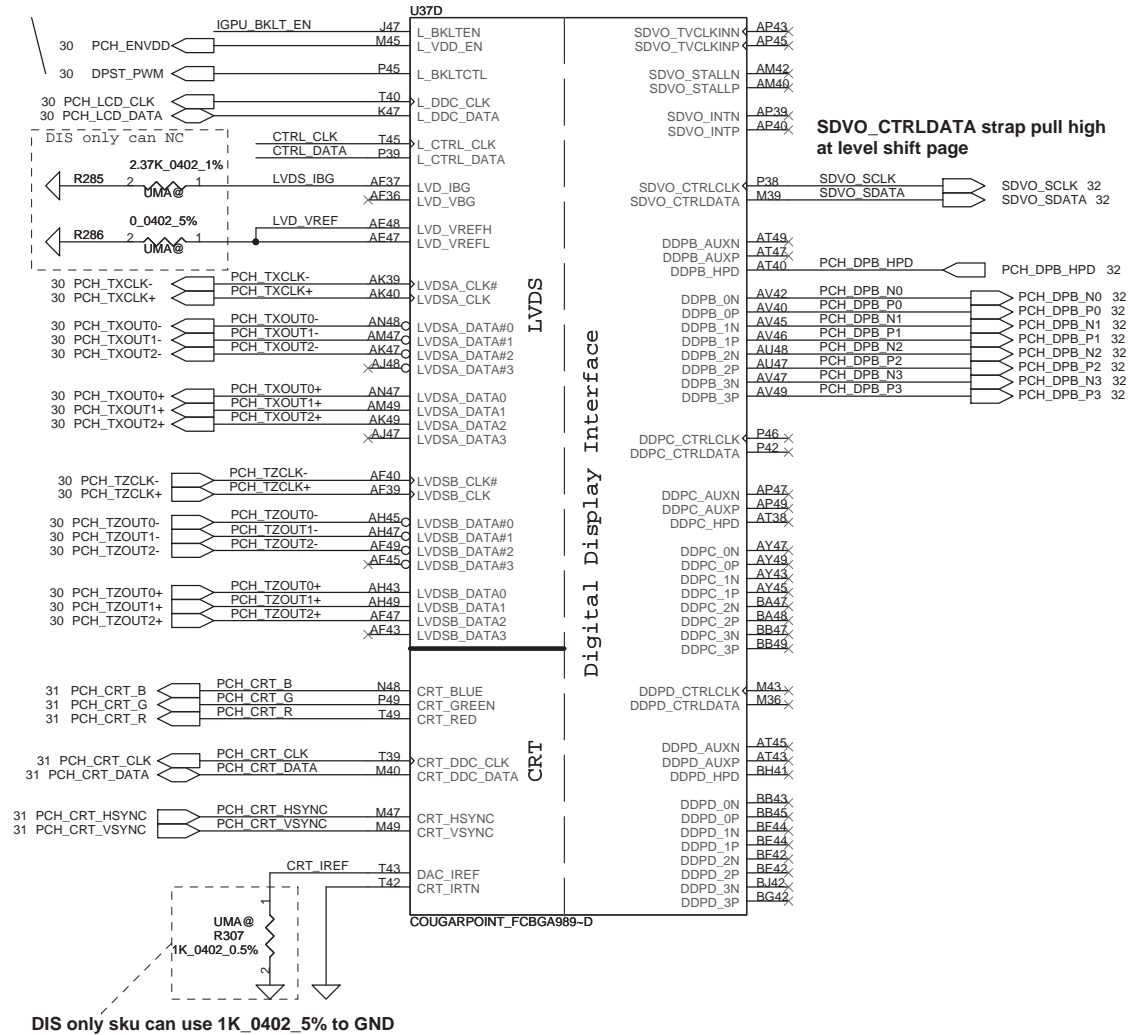
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								Document Number		4019A9		Rev B	
								Date: Tuesday, November 09, 2010		Sheet 15 of 60			



**LVDS disable:**  
DATA/Clock/Control an NC  
VCC\_TX\_LVDS,VCCA\_LVDS PD to GND

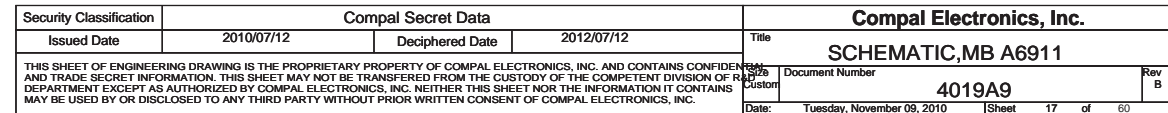
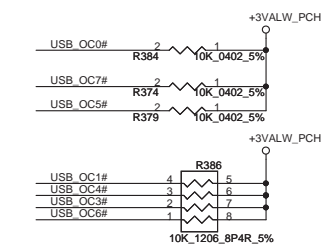
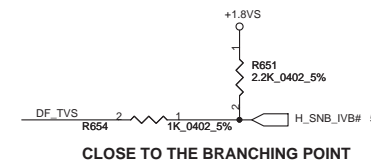
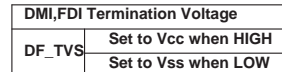
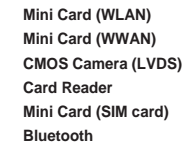
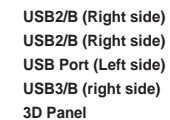
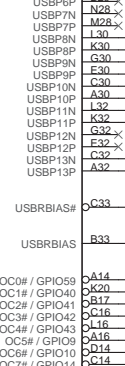
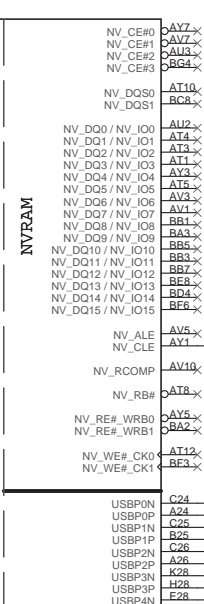
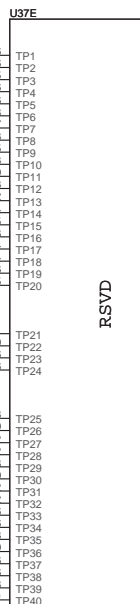
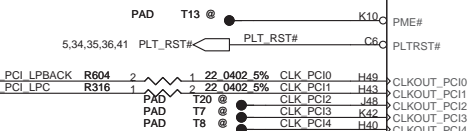
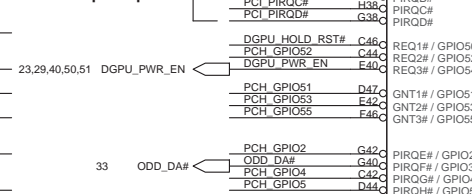
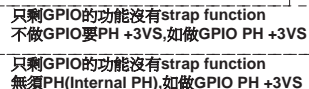
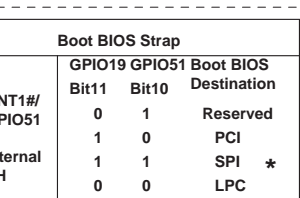
**CRT disable:**  
DATA/Clock/Control an NC  
VCCADAC connect to +3VS

Pull high at LVDS conn side.

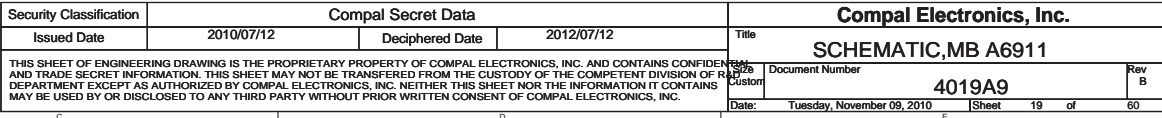


DIS only sku can use 1K\_0402\_5% to GND

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				Date:	Tuesday, November 09, 2010
				Sheet	16 of 60

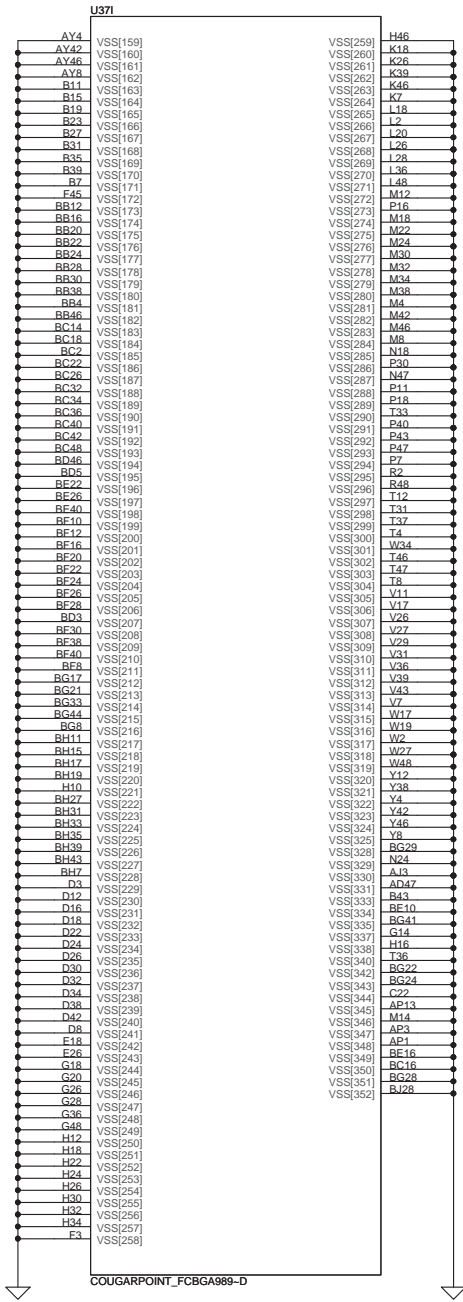
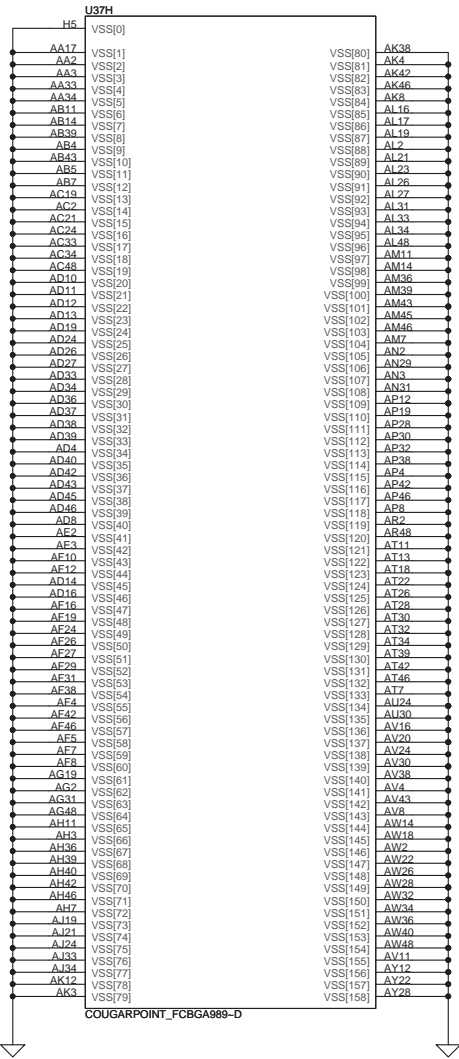












[illegible]

- Controls panel digital power on/off
- Active High ,external PD need

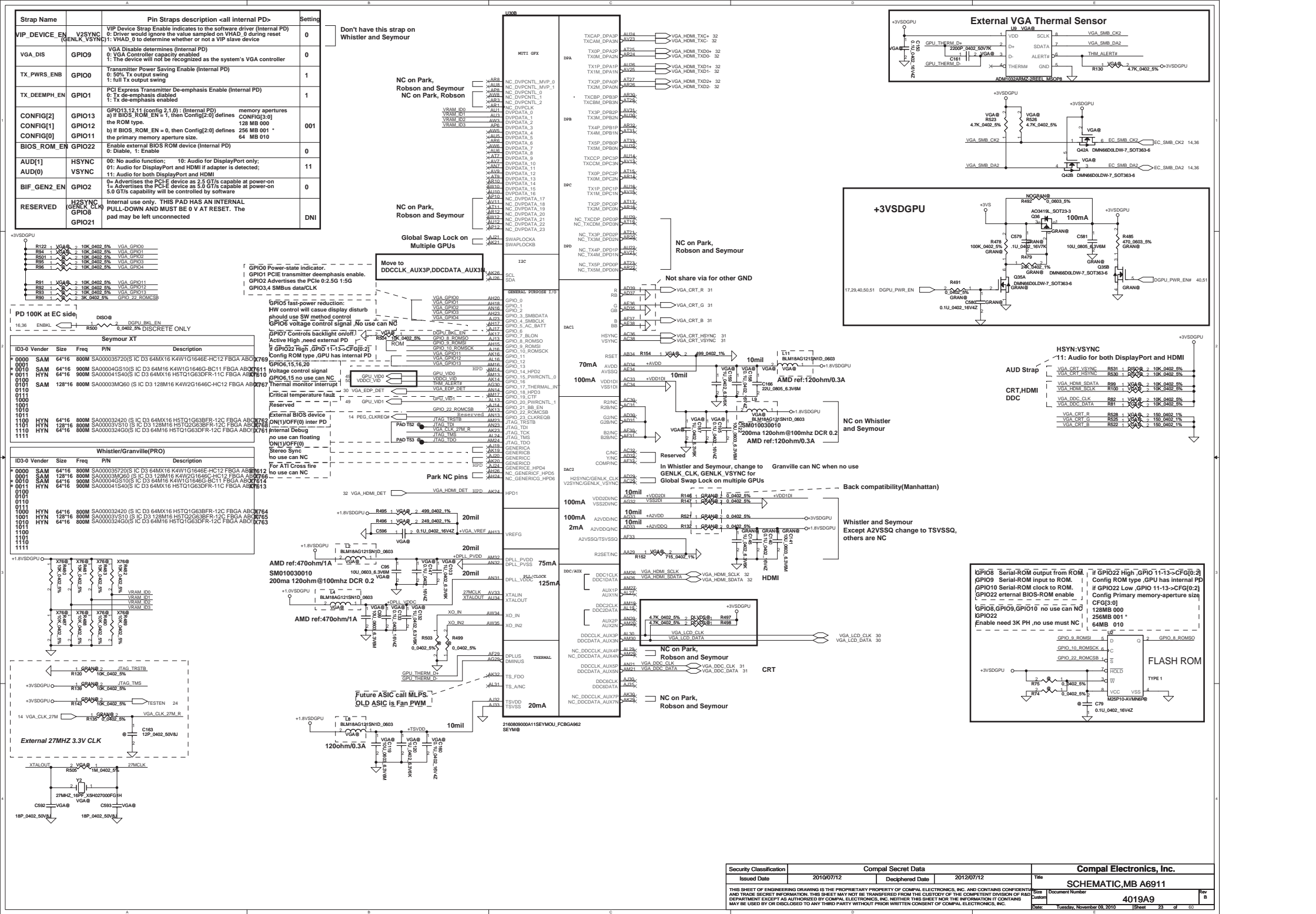
### Display Port E config

DPO

SEYM@

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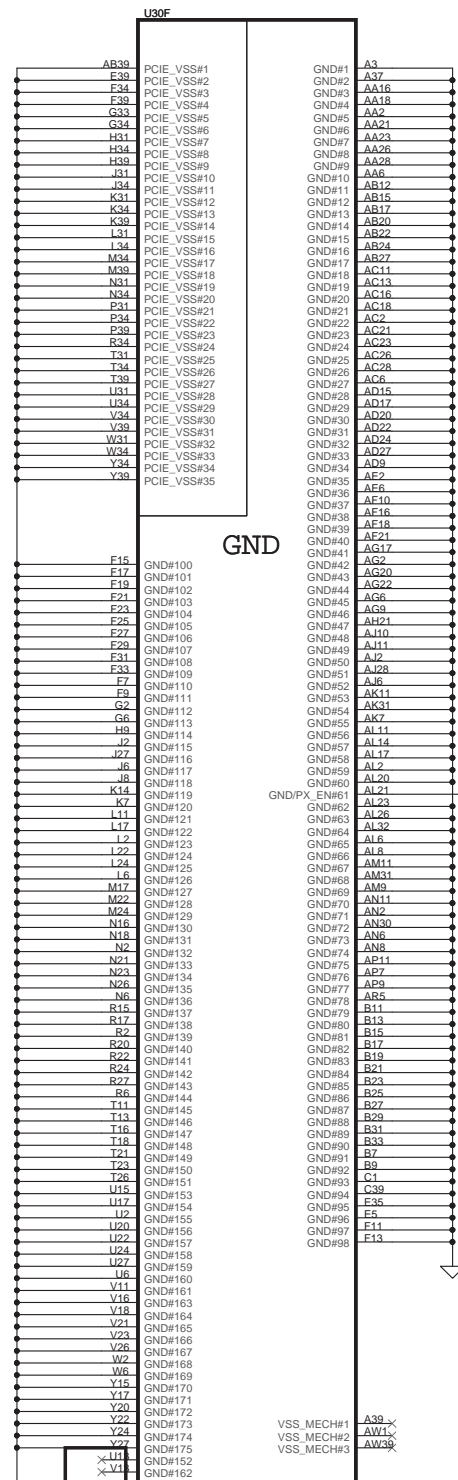
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				Custom	4019A9		
				Date:	Tuesday, November 09, 2010	Sheet	22 of 60







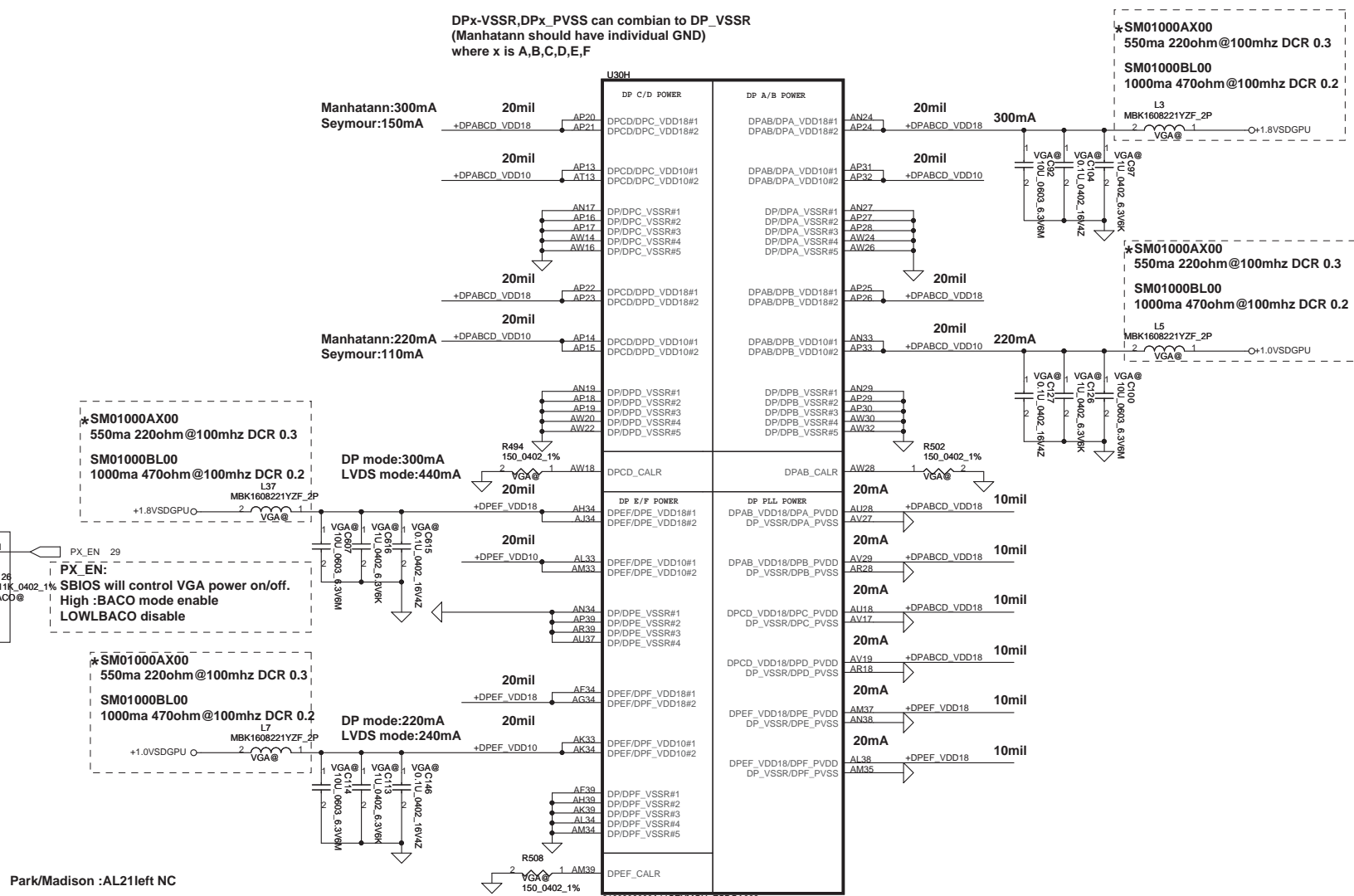




DPA\_VDD18,DPA\_PVDD,DPB\_VDD18,DPB\_PVDD  
can combian to DPAB\_VDD18  
DPC\_VDD18,DPC\_PVDD,DPD\_VDD18,DPD\_PVDD  
can combian to DPCD\_VDD18  
(DPD\_VDD18,DPD\_PVDD not applicable on Robson/Park)  
DPE\_VDD18,DPE\_PVDD,DPF\_VDD18,DPF\_PVDD  
can combian to DPEF\_VDD18

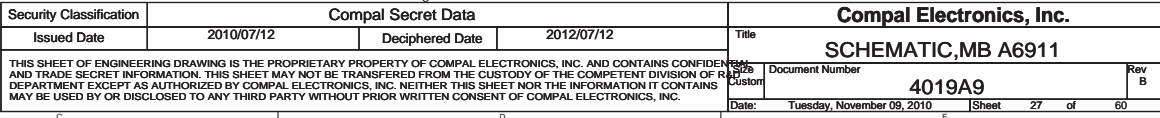
DPx\_VSSR,DPx\_PVSS can combian to DP\_VSSR  
(Manhattan should have individual GND)  
where x is A,B,C,D,E,F

Seymour/Whistler :  
DPA\_VDD10,DPB\_VDD10  
can combian to DPAB\_VDD10  
DPC\_VDD10,DPD\_VDD10  
can combian to DPCD\_VDD10  
DPE\_VDD10,DPD\_VDD10  
can combian to DPEF\_VDD10

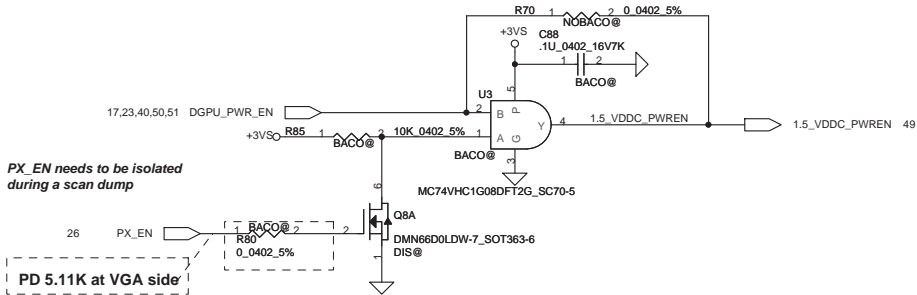


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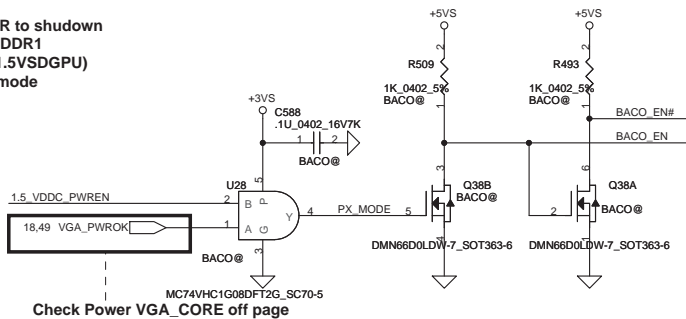






PX\_EN = 1, For BACO Mode  
PX\_EN = 0, For Normal Mode

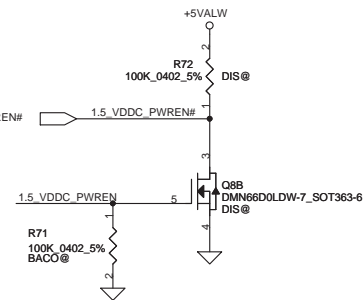
PX\_EN:  
Connect to PWR to shutdown  
VDDC/VDDCI/VDDR1  
(VGA\_CORE, +1.5VSDGPU)  
High in BACO mode



BACO\_EN#=1 (BACO mode)  
BACO\_EN#=0 (Normal mode)  
BACO\_EN=0 (BACO mode)  
BACO\_EN=1 (Normal mode)

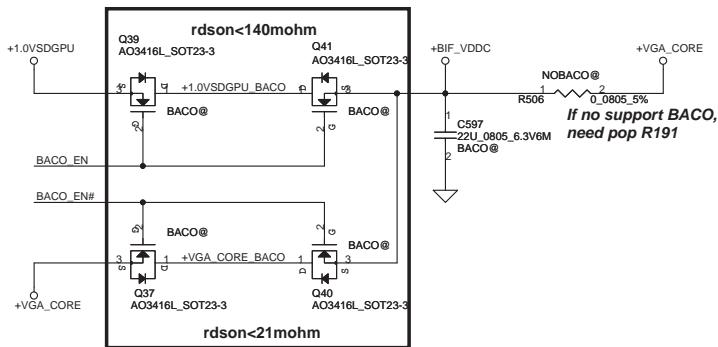
BACO\_EN/BACO\_EN#:  
0: BACO Mode->BACO\_EN High->  
BIF\_VDDC=+1.0VSDGPU(N-MOS), VGA\_CORE(P-MOS)

1: Normal mode->BACO\_EN# High->  
BIF\_VDDC=+VGA\_CORE(N-MOS), VGA\_CORE(N-MOS)



VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU

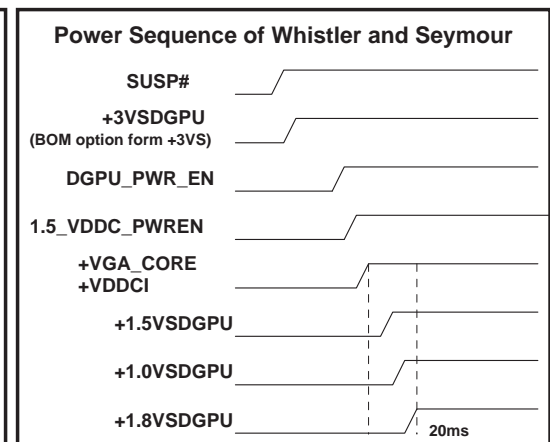
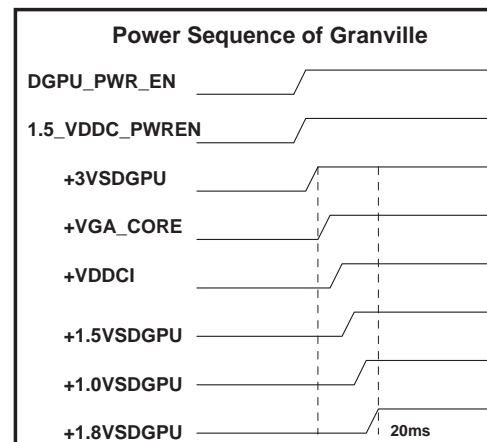
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN



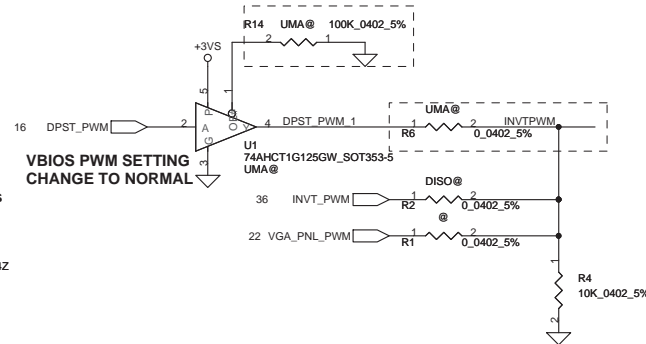
PX\_EN = 1, For BACO Mode  
BACO\_EN=0  
BACO\_EN#=1(5V) => BIF\_VDDC=+1.0VSDGPU  
PX\_EN = 0, For Normal Mode  
BACO\_EN=1(5V) => BIF\_VDDC=VGA\_CORE  
BACO\_EN#=0

For the MOSFETs on the path of delivering  
PCIE\_VDDC(+1.0VSDGPU) to  
BIF\_VDDC Rds(on) of 140 mOhms or less is required.

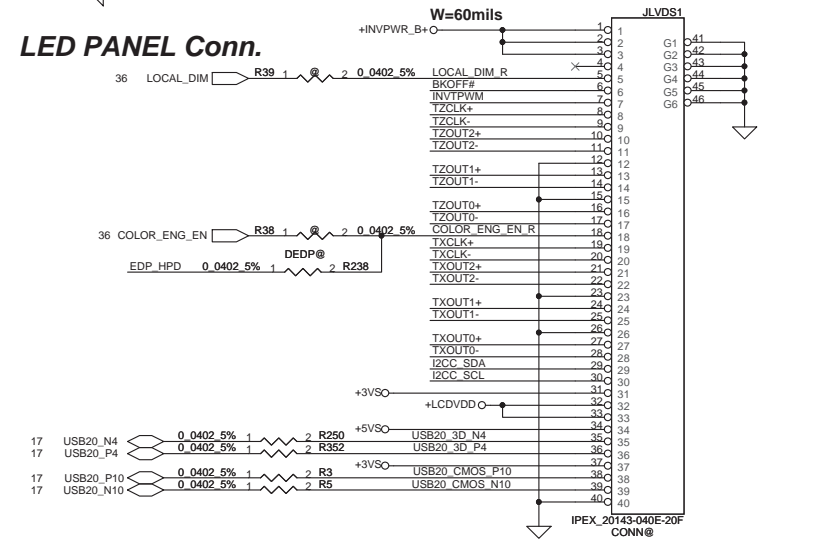
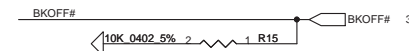
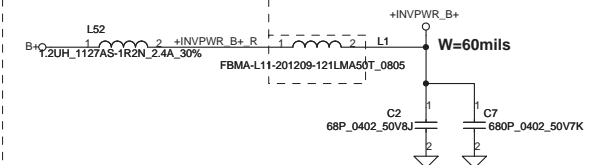
For the MOSFETs on the path of delivering VGA\_CORE to  
BIF\_VDDC, Rds(on) of 21 mOhms or less is required.



## LCD POWER CIRCUIT



SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



The schematic shows a +3VS supply connected to two pins, R8 and R10, each through a 100K\_0402\_5% resistor. R8 is labeled I2C\_SDA and R10 is labeled I2C\_SCL. Both pins are also connected to a DEDP@ signal line.

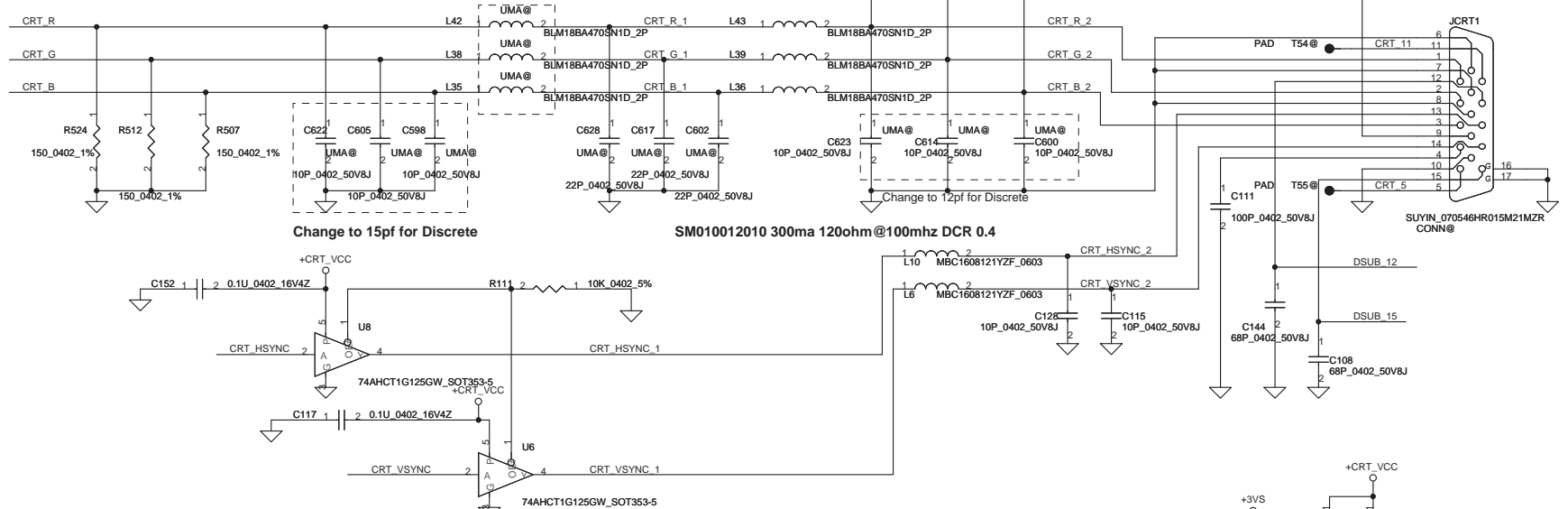
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# CRT Connector

CRB1.0 use 47ohm@100Mhz Bead

SM01000GA00 300mA 47ohm@100Mhz DCR 0.55

Change to 0 ohm for Discrete



## UMA only/Muxless

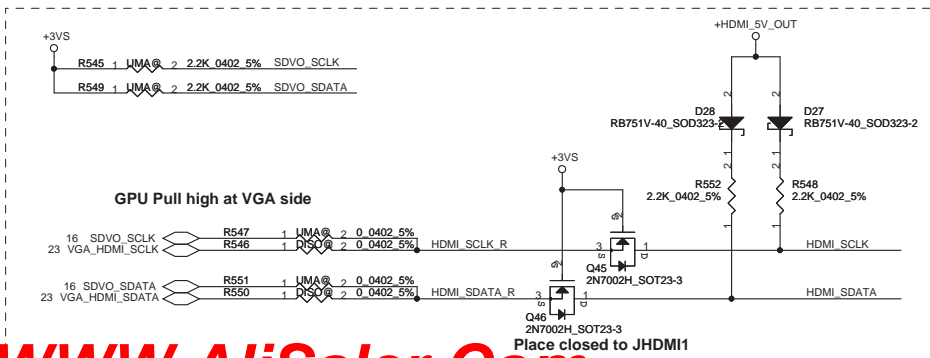
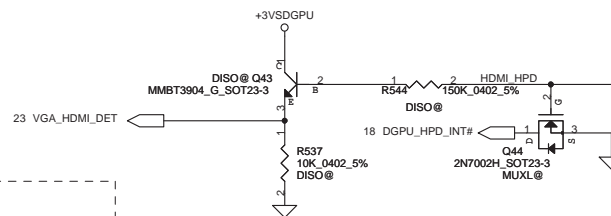
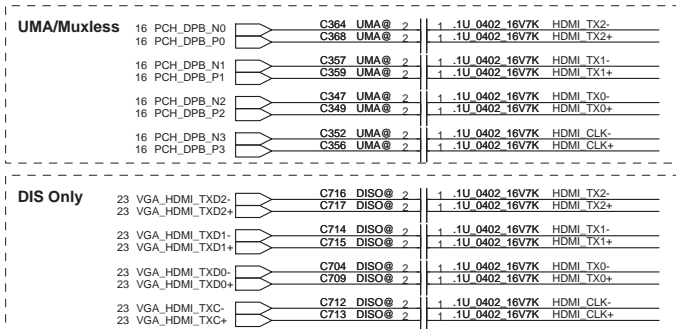
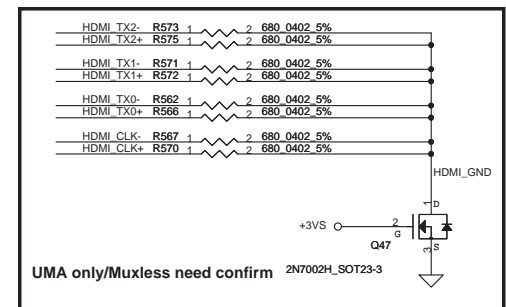
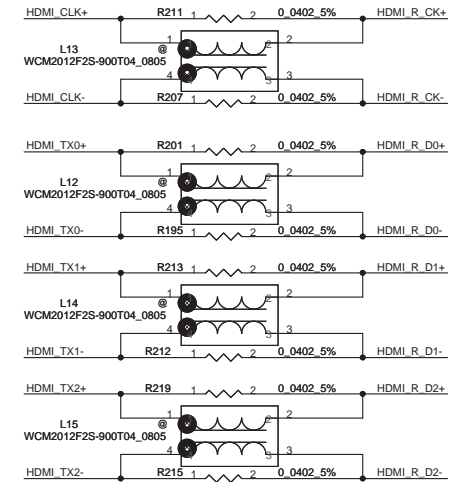
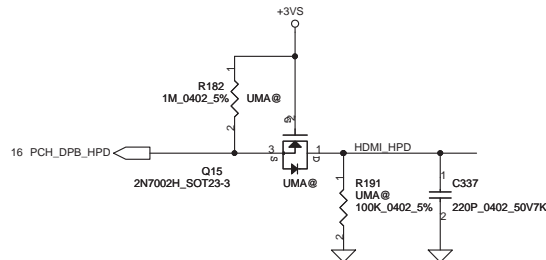
16	PCH_CRT_R	PCH CRT R	R529	UMA	1	0.0402 5%	CRT R
16	PCH_CRT_G	PCH CRT G	R519	UMA	1	0.0402 5%	CRT G
16	PCH_CRT_B	PCH CRT B	R511	UMA	1	0.0402 5%	CRT B
16	PCH_CRT_HSYNC	PCH CRT HSYNC	R137	UMA	1	33.0402 5%	CRT HSYNC
16	PCH_CRT_VSYNC	PCH CRT VSYNC	R110	UMA	1	33.0402 5%	CRT VSYNC
16	PCH_CRT_CLK	PCH CRT CLK	R102	UMA	1	0.0402 5%	CRT DDC CLK
16	PCH_CRT_DATA	PCH CRT DATA	R89	UMA	1	0.0402 5%	CRT DDC DATA

PCH DDC PU 2.2K on Page 17

## Discrete only

23	VGA_CRT_R	VGA CRT R	R527	DISOR	1	0.0402 5%	CRT R
23	VGA_CRT_G	VGA CRT G	R514	DISOR	1	0.0402 5%	CRT G
23	VGA_CRT_B	VGA CRT B	R510	DISOR	1	0.0402 5%	CRT B
23	VGA_CRT_HSYNC	VGA CRT HSYNC	R131	DISOR	1	0.0402 5%	CRT HSYNC
23	VGA_CRT_VSYNC	VGA CRT VSYNC	R107	DISOR	1	0.0402 5%	CRT VSYNC
23	VGA_DDC_CLK	VGA DDC CLK	R98	DISOR	1	0.0402 5%	CRT DDC CLK
23	VGA_DDC_DATA	VGA DDC DATA	R86	DISOR	1	0.0402 5%	CRT DDC DATA

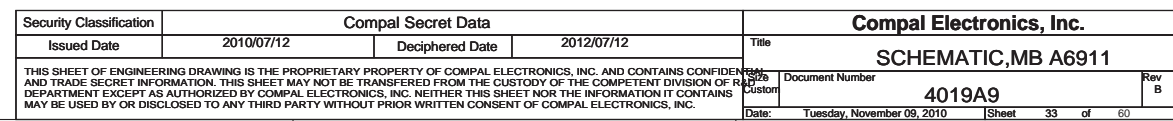
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Schematic, MB A6911	
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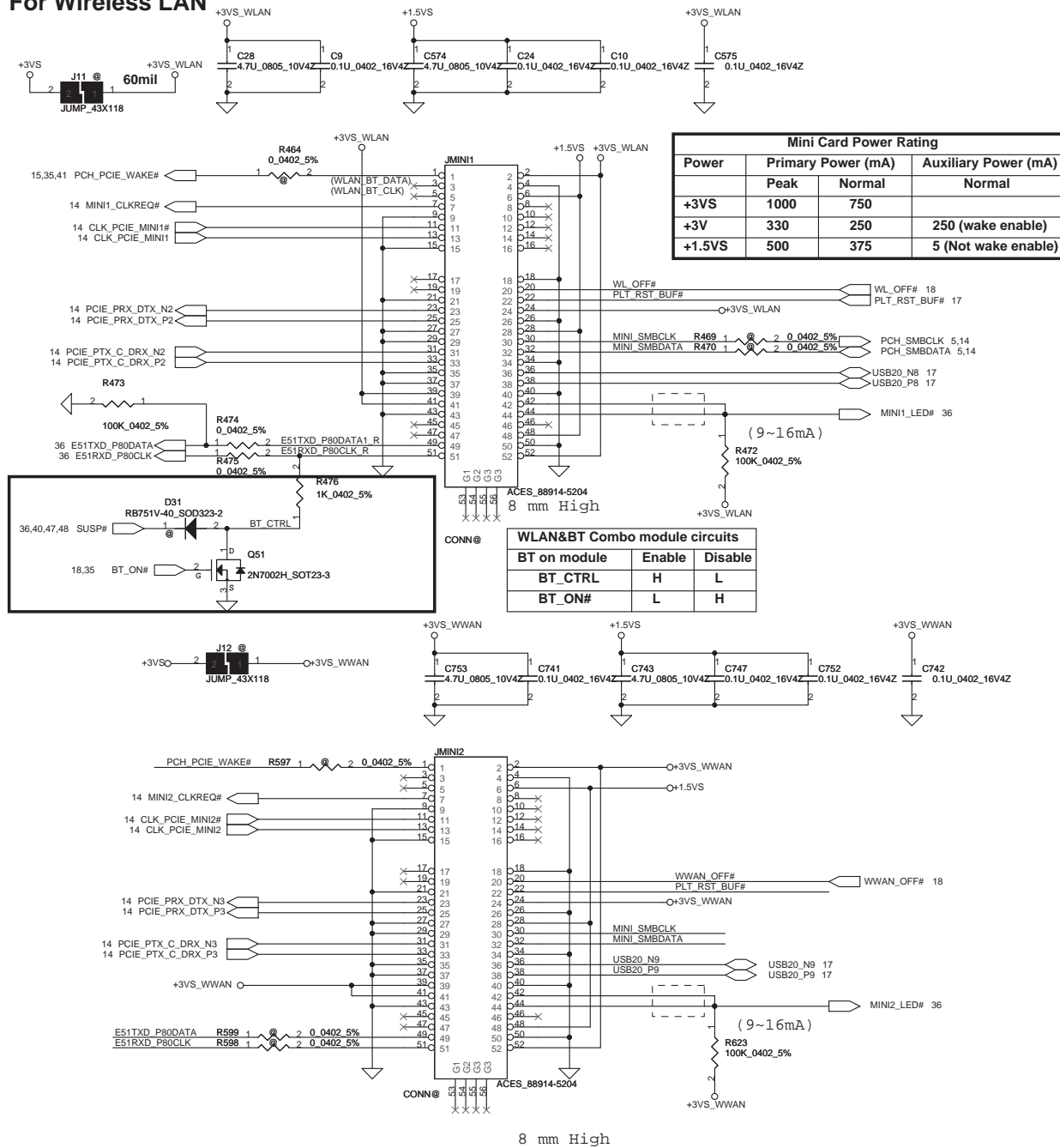
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2010/07/12		Deciphered Date		2012/07/12		Title		SCHEMATIC,MB A6911			
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								Customer		4019A9			
Date:				Tuesday, November 09, 2010				Sheet		32 of 60			



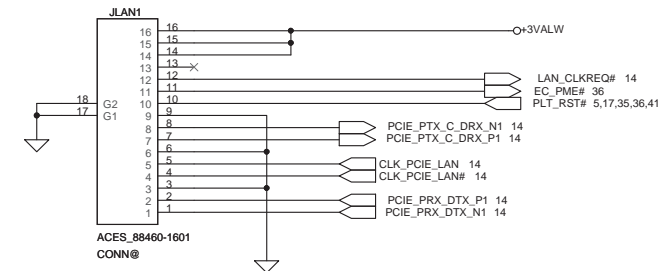
## CL 2.9 mm

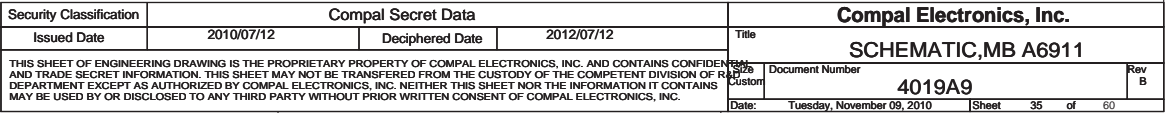
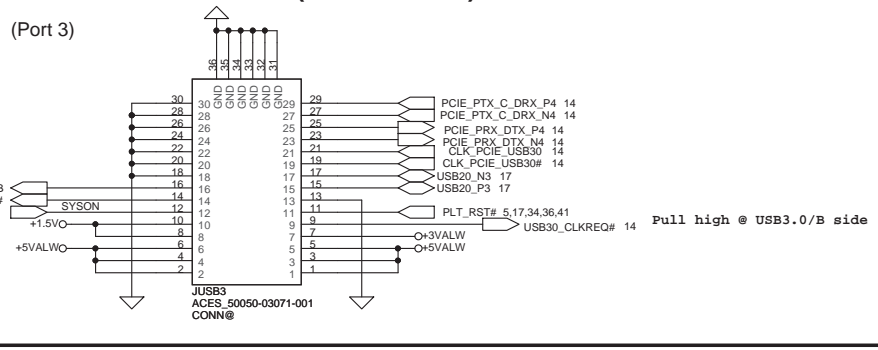
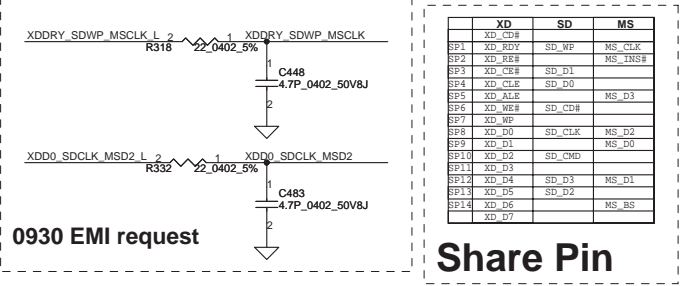
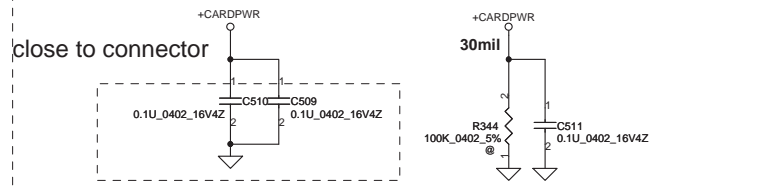


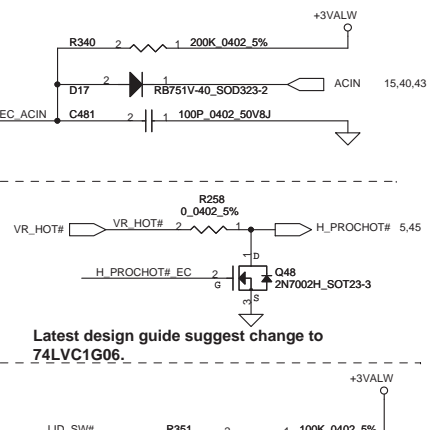
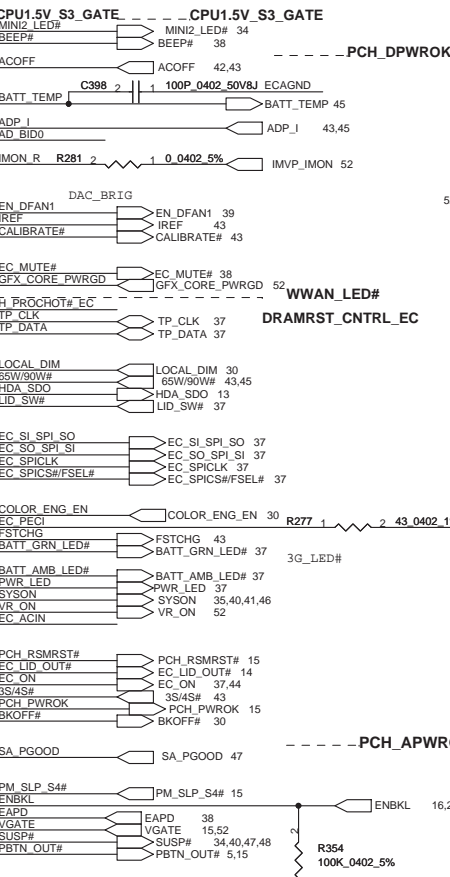
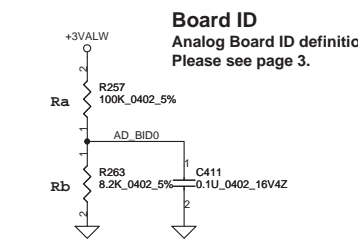
# For Wireless LAN



## LAN CONN. LS-6912P



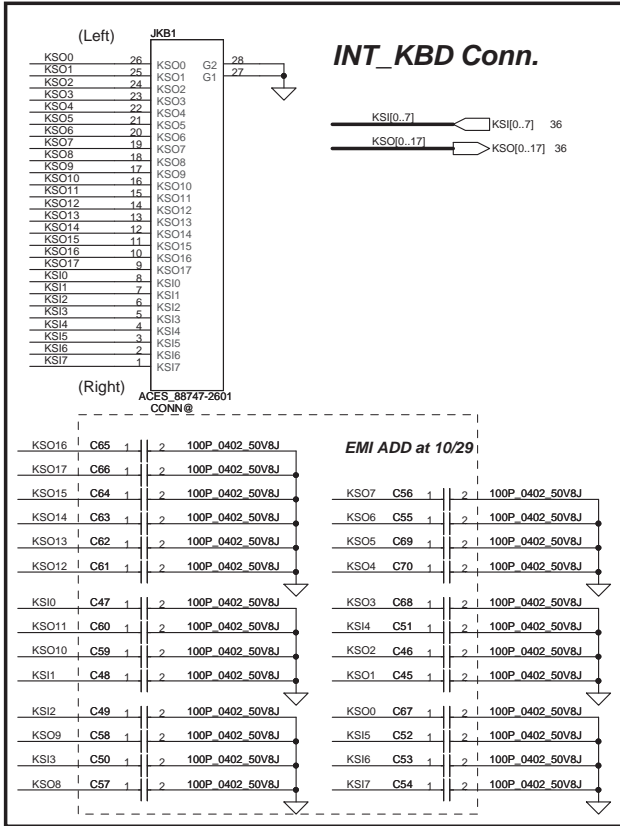
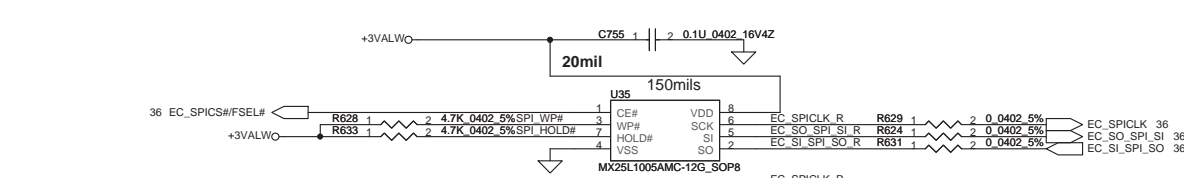




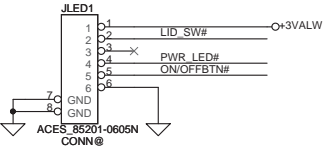
*Place on RAM door*



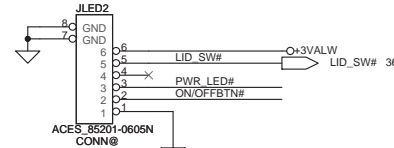
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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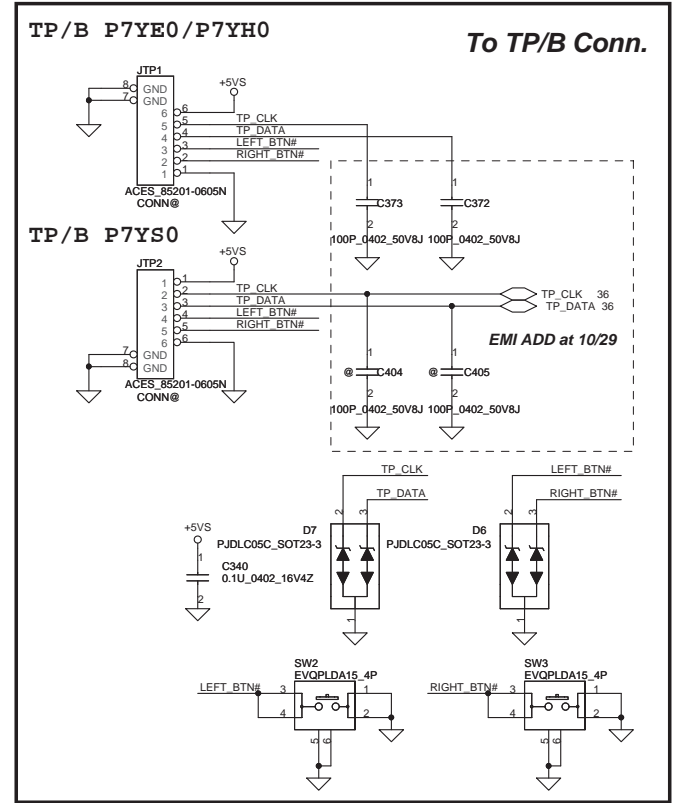
### LED/B P7YE0/P7YH0 LS-6913P



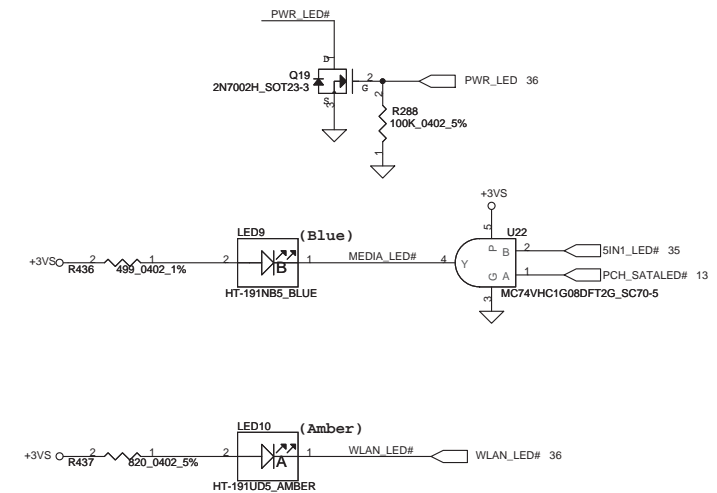
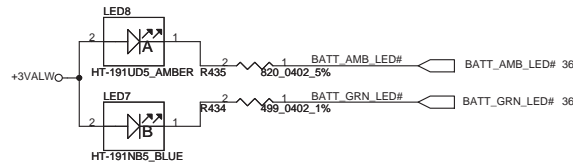
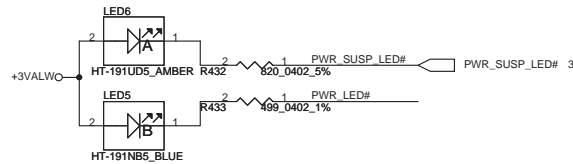
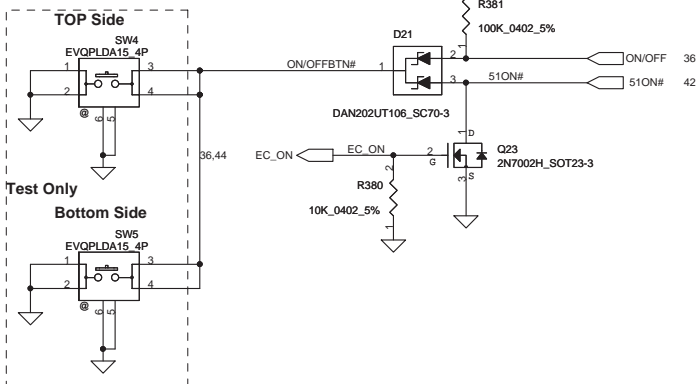
### LED/B P7YS0 LS-6913P



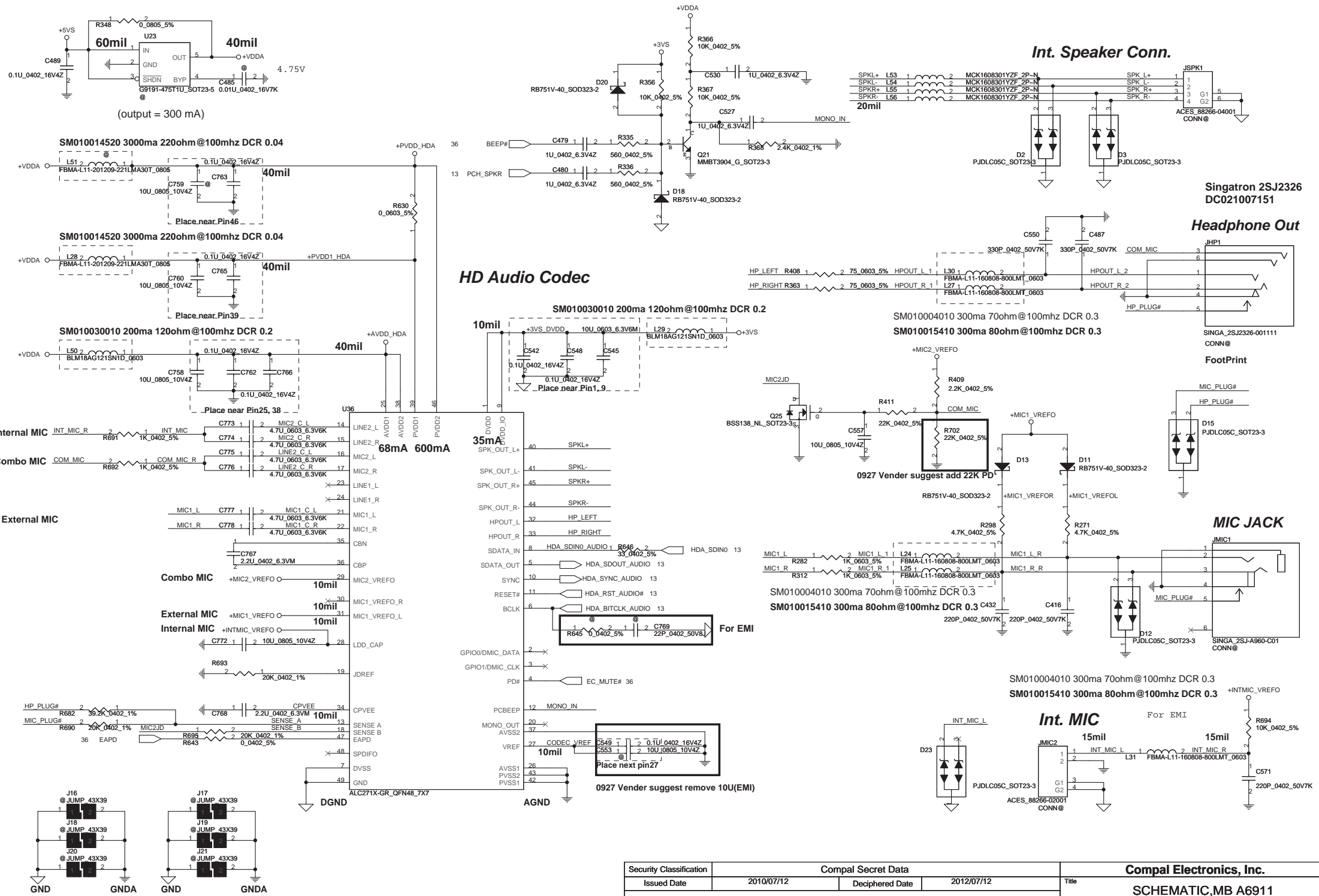
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue		Blue	Amber		



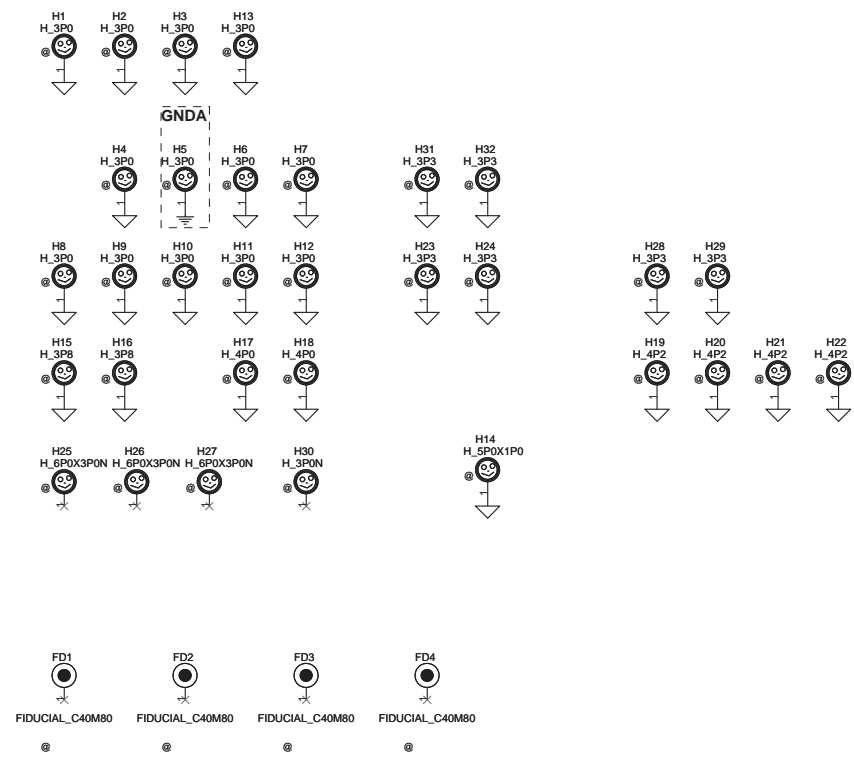
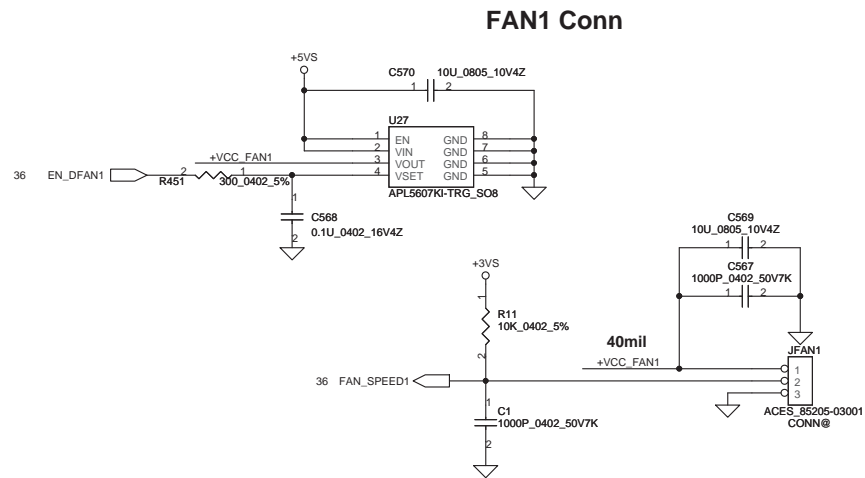
### Power Button ON/OFF switch



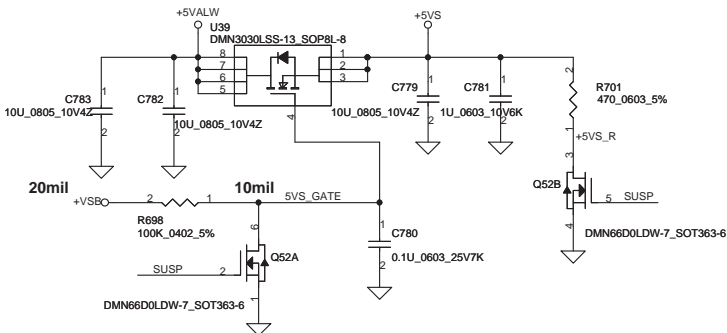




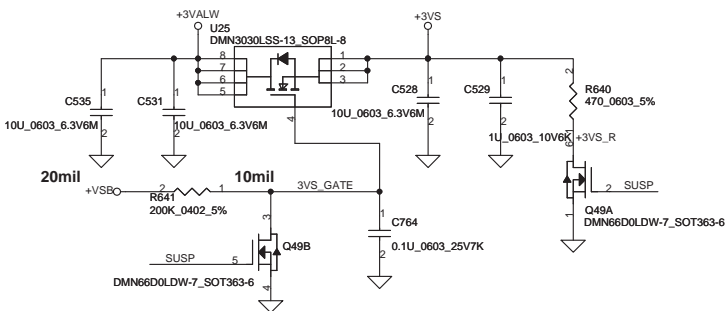
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		Deciphered Date		2012/07/12	
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### +5VALW TO +5VS

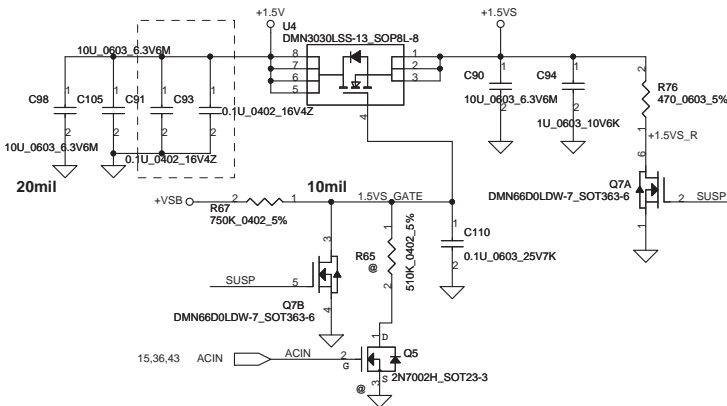


### +3VALW TO +3VS

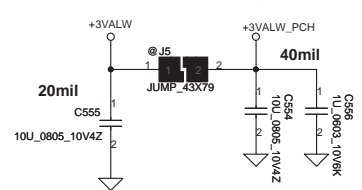


### +1.5V to +1.5VS

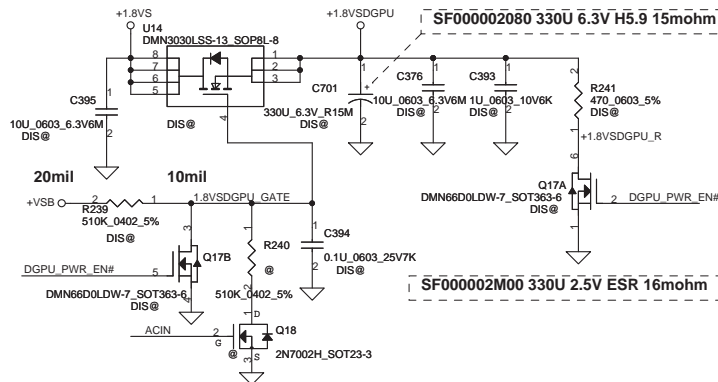
1211 EMI ADD 0.1U close PJ5



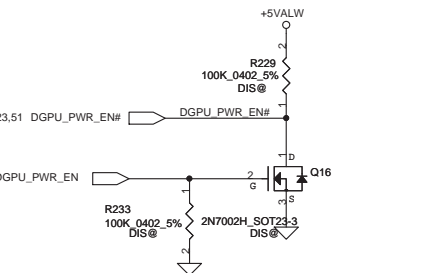
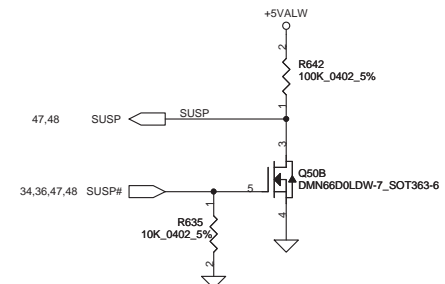
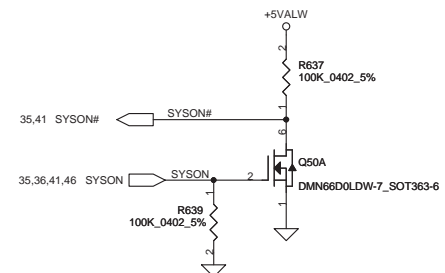
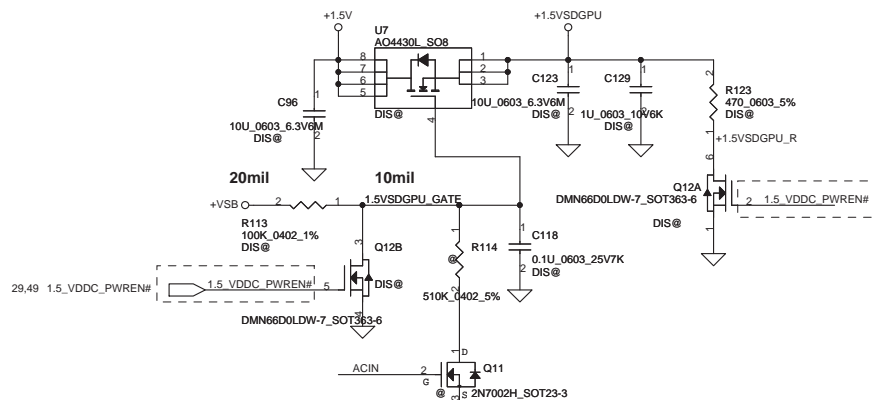
### +3VALW TO +3VALW(PCH AUX Power)



### +1.8VS to +1.8VSDGPU for GPU



### +1.5V to +1.5VSDGPU for GPU



2009/08/14

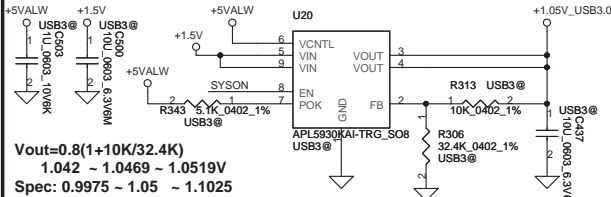
CP\_S3PowerReduction  
WhitePaper\_Rev0.9

0.5VS need to discharge

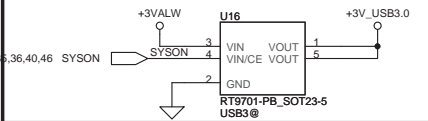
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WWW.AllSaler.Com

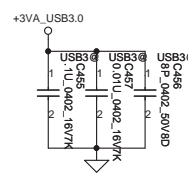
## +1.5V to +1.05V Transfer



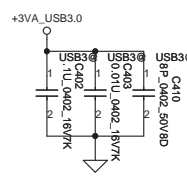
## +3VALW to +3V Transfer



## Close to U41.D7

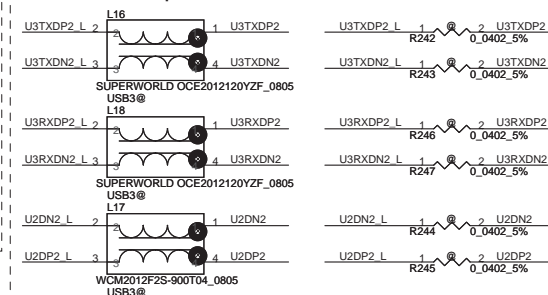


## Close to U41.P13

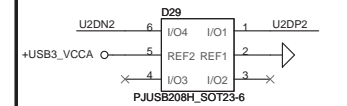


7K for customer request, can use other kind of capacitor, like Y5V.

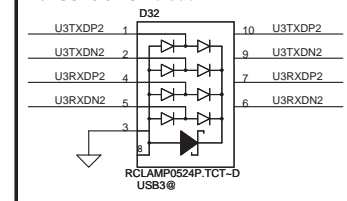
## For EMI request



## For USB2.0 ESD diode



## For USB3.0 ESD diode



SPEC Max: +3V---200mA; +1.05V---800mA

Idle mode: 0.489W

+3V---43mA; +1.05V---328mA

D3 mode: 0.066W

+3V---5.4mA; +1.05V---45mA

Can be attach to EC, either.

PCI Express/ExpressCard select signal  
1: others  
0: Express Card or Mini card

As short as possible

SF000002Y00 220U  
6.3V 17mohm H4.5

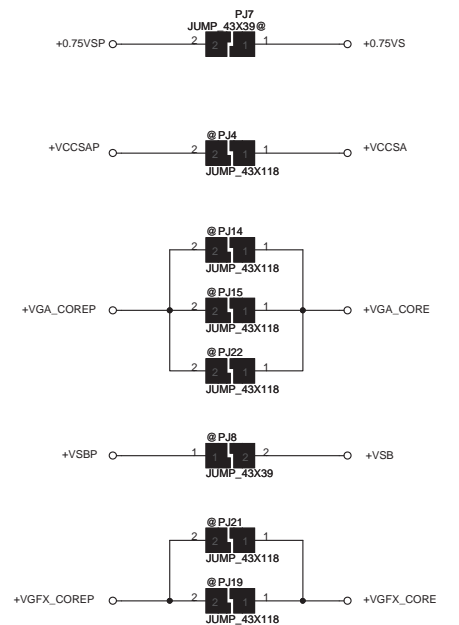
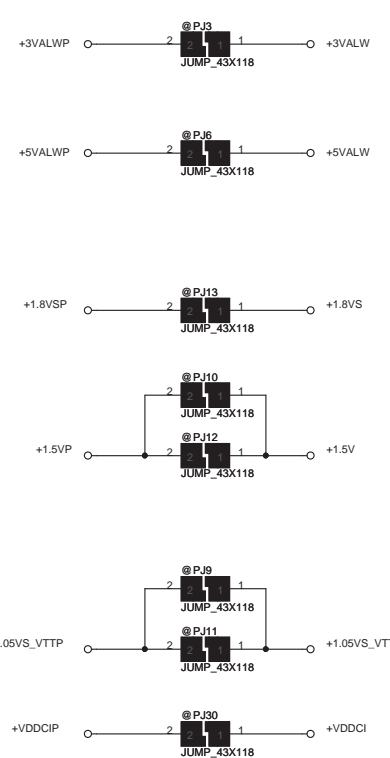
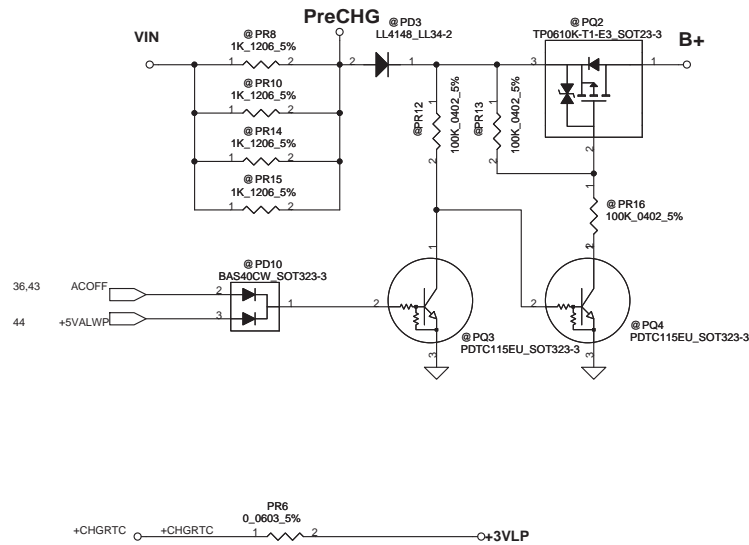
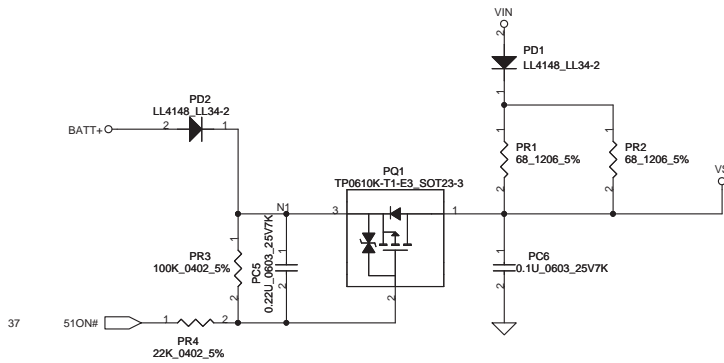
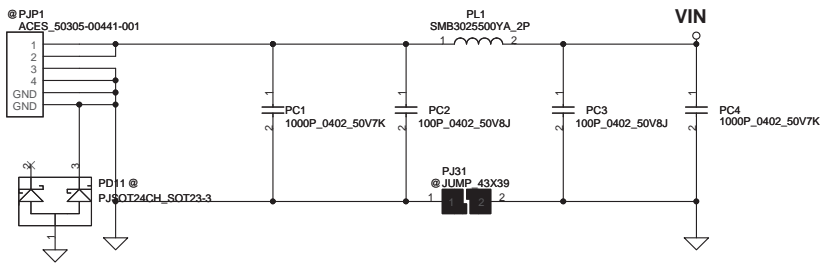
Resistor overlap with L70  
USB2.0 Conn SKU

USB2.0 Conn

Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y5,R816,C879,C880
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

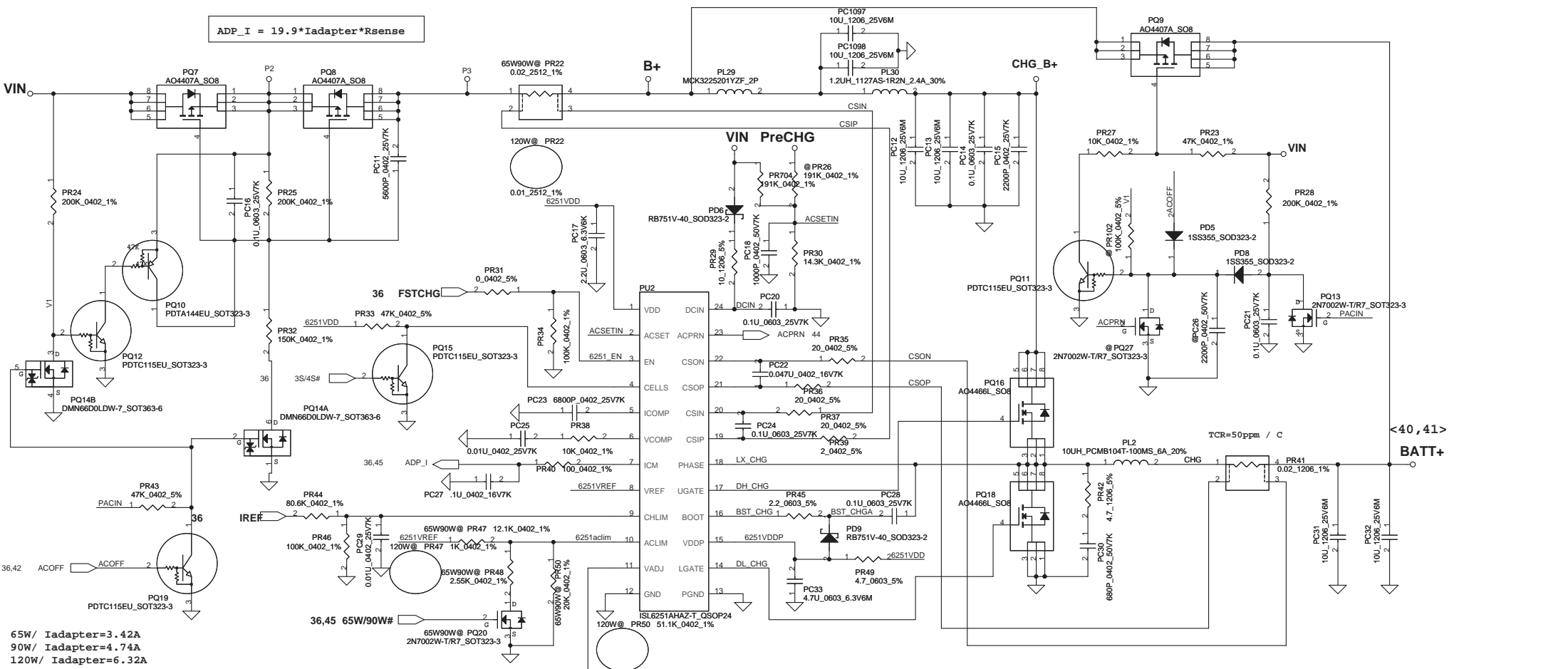
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ADP\_I = 19.9\*Iadapter\*Rsense

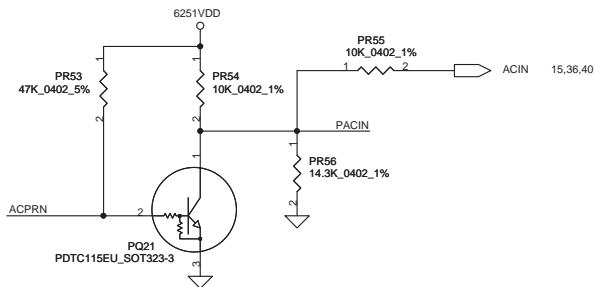


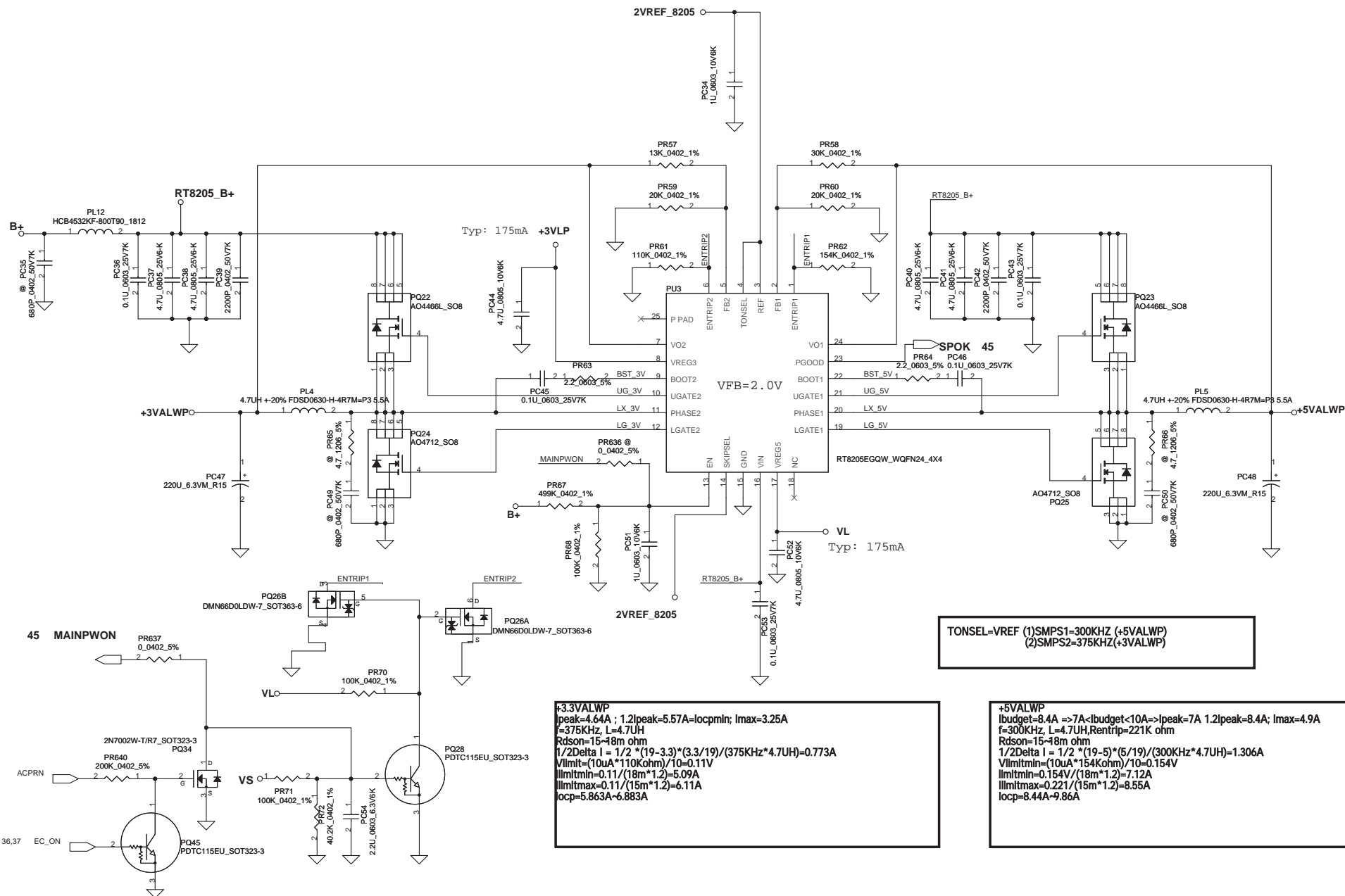
65W/ Iadapter=3.42A  
90W/ Iadapter=4.74A  
120W/ Iadapter=6.32A

**CP mode, for Acer spec, CP=0.85\*Iadapter.**  
For 90W, 65W/90W#=Low, Vref=2.39V  
Iinput=(1/0.02)(0.05\*Vaclm/2.39+0.05)  
where Vaclm=1.489V, Iinput=4.05A  
For 65W, 65W/90W#=#High  
Iinput=(1/0.02)(0.05\*Vaclm/2.39+0.05)  
where Vaclm=0.376, Iinput=2.89A.  
For 120W  
Iinput=(1/0.01)(0.05\*Vaclm/2.39+0.05)  
Vaclm=2.344V, Iinput=5.403

BATT Type	Charging Voltage (0x15)	CV mode	CC=0.6~4.48A
Normal 3S LI-ON Cells	12600mV	12.60V	IREF=0.7224*Icharge IREF=0.43V~3.24V

Kv  
Rinternal ic=514K Rec=3K R1=PR379=15.4K  
R2=PR381=31.6K  
R=514K//31.6K/(15.4K+3K)=11.372K  
r=514K//514K//31.6K=28.14K  
Vocell=0.175\*Vadj+3.99V  
4.2V=0.175\*Vadj+3.99V =>Vadj=1.2V  
Vadj=Vref\*(R/(R+514K))+CALIBRATE\*(r/(r+514K))  
1.1483=CALIBRATE\*0.6046 =>CALIBRATE=1.899  
1.899=(4.2-(Vocell+A\*0.175))\*Kv=(4.2-(4.2+A\*0.175))\*Kv  
A=Vref\*(R/(R+514K))=0.052  
Kv=9.451  
Kvlim=Iref\*(PR46/(PR44+PR46))  
=Iref\*(100K/(80.6K+100K))  
=Iref\*0.5537  
Icharge=(165mV/PR22)\*(Vchlim/3.3V)  
=(165m/20m)\*(1/3.3V)\*Iref\*0.5537  
=1.3842\*Iref  
Iref=0.7224\*Icharge =>Ki=0.7224



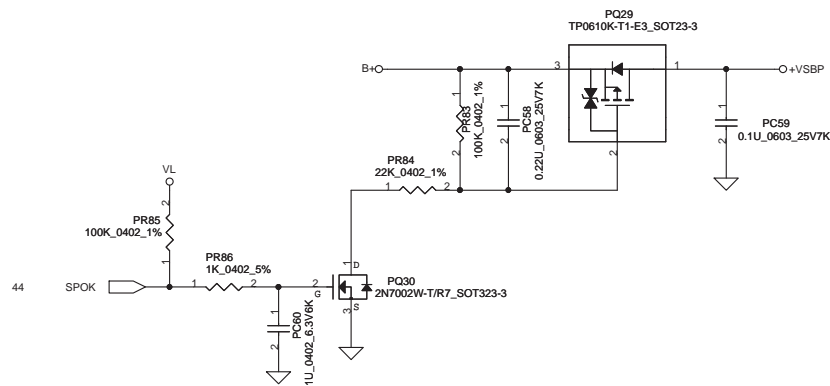
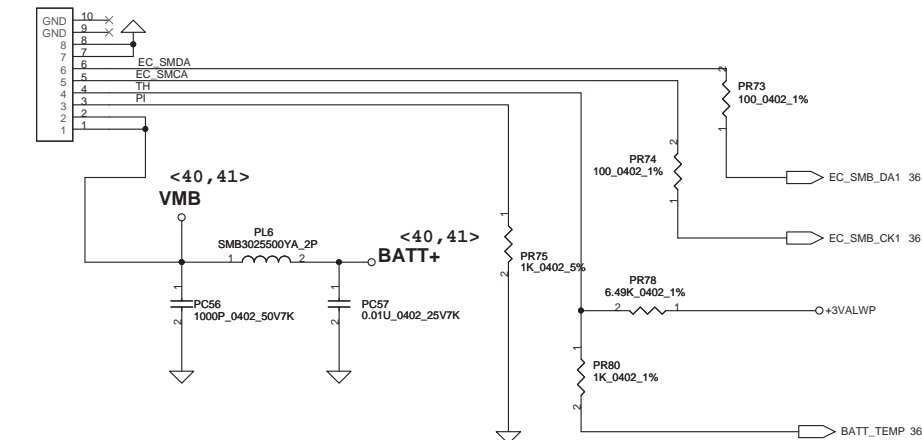


TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)  
(2)SMPS2=375KHZ(+3VALWP)

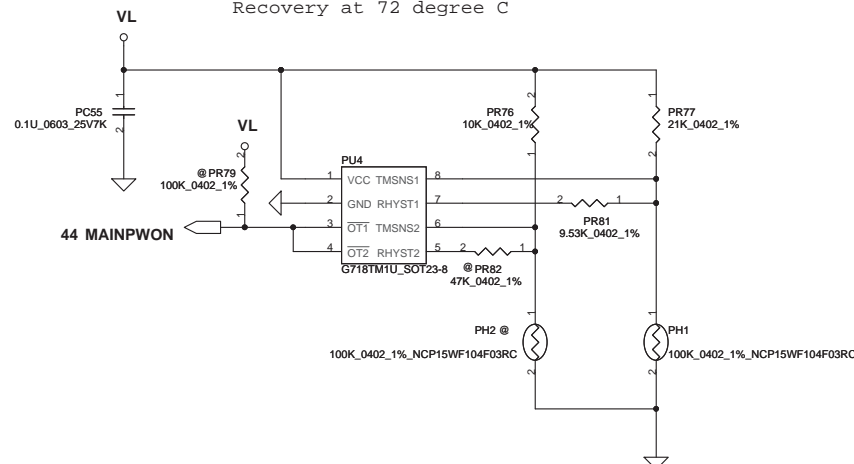
**3.3VALWP**  
Ipeak=4.64A ; 1.2Ipeak=5.57A=Iocpmin; Imax=3.25A  
f=375KHz, L=4.7UH  
Rdson=15-48m ohm  
1/2Delta I = 1/2 \* (19-3.3) \* (3.3/19) / (375KHz \* 4.7UH) = 0.773A  
Vlimtmin=(10uA\*110Kohm)/10=0.11V  
Ilimtmin=0.11/(18m\*1.2)=5.09A  
Ilimtmax=0.11/(15m\*1.2)=6.11A  
Iocp=5.863A~6.883A

**+5VALWP**  
Ibudget=8.4A => 7A<Ibudget<10A=>Ipeak=7A 1.2Ipeak=8.4A; Imax=4.9A  
f=300KHz, L=4.7UH, Rentrip=221K ohm  
Rdson=15-48m ohm  
1/2Delta I = 1/2 \* (19-5) \* (5/19) / (300KHz \* 4.7UH) = 1.306A  
Vlimtmin=(10uA\*154Kohm)/10=0.154V  
Ilimtmin=0.154V/(18m\*1.2)=7.12A  
Ilimtmax=0.221/(15m\*1.2)=8.55A  
Iocp=8.44A~9.86A

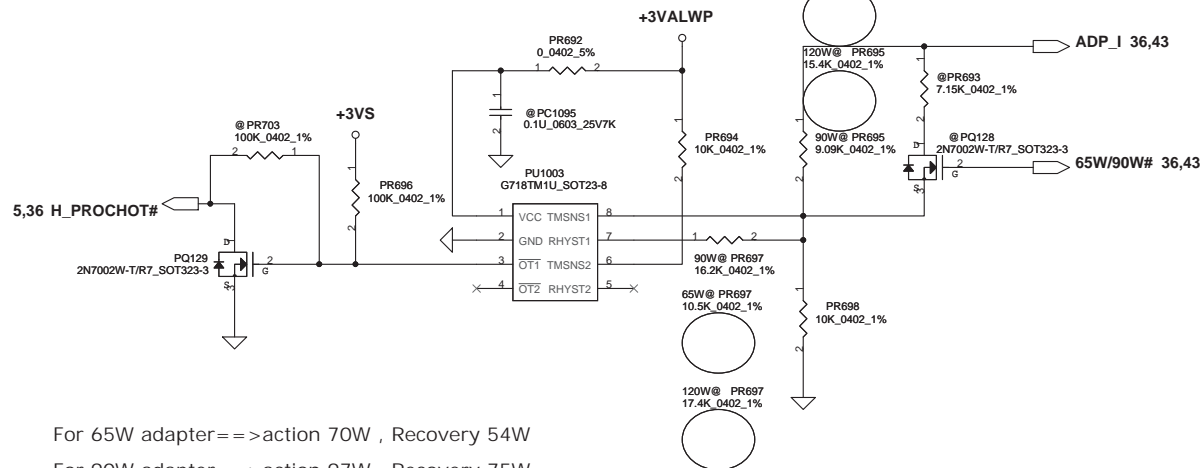
© PJP2  
SUYIN\_200275GR008G13GZR



PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 72 degree C



Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W  
For 90W adapter==>action 97W , Recovery 75W  
For 120W adapter==>action 135W , Recovery 100W

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35,36,40,41 SYSON

+5VALW

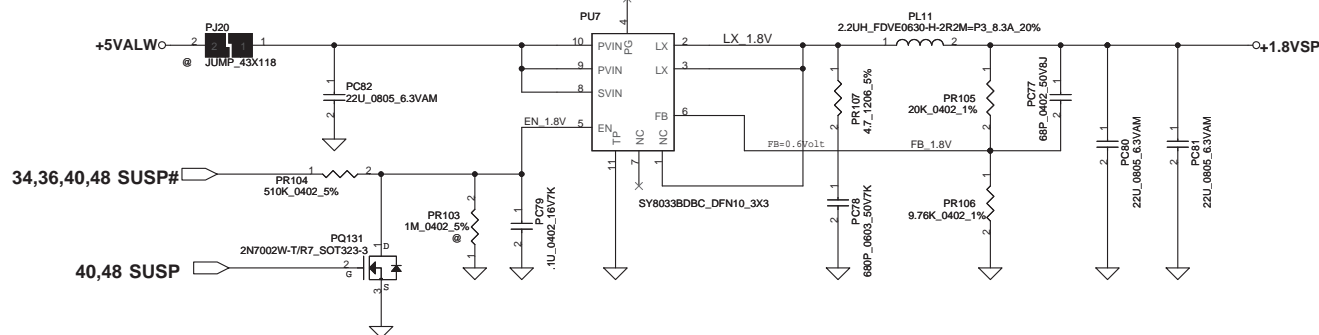
+5VALW

+1.5VP

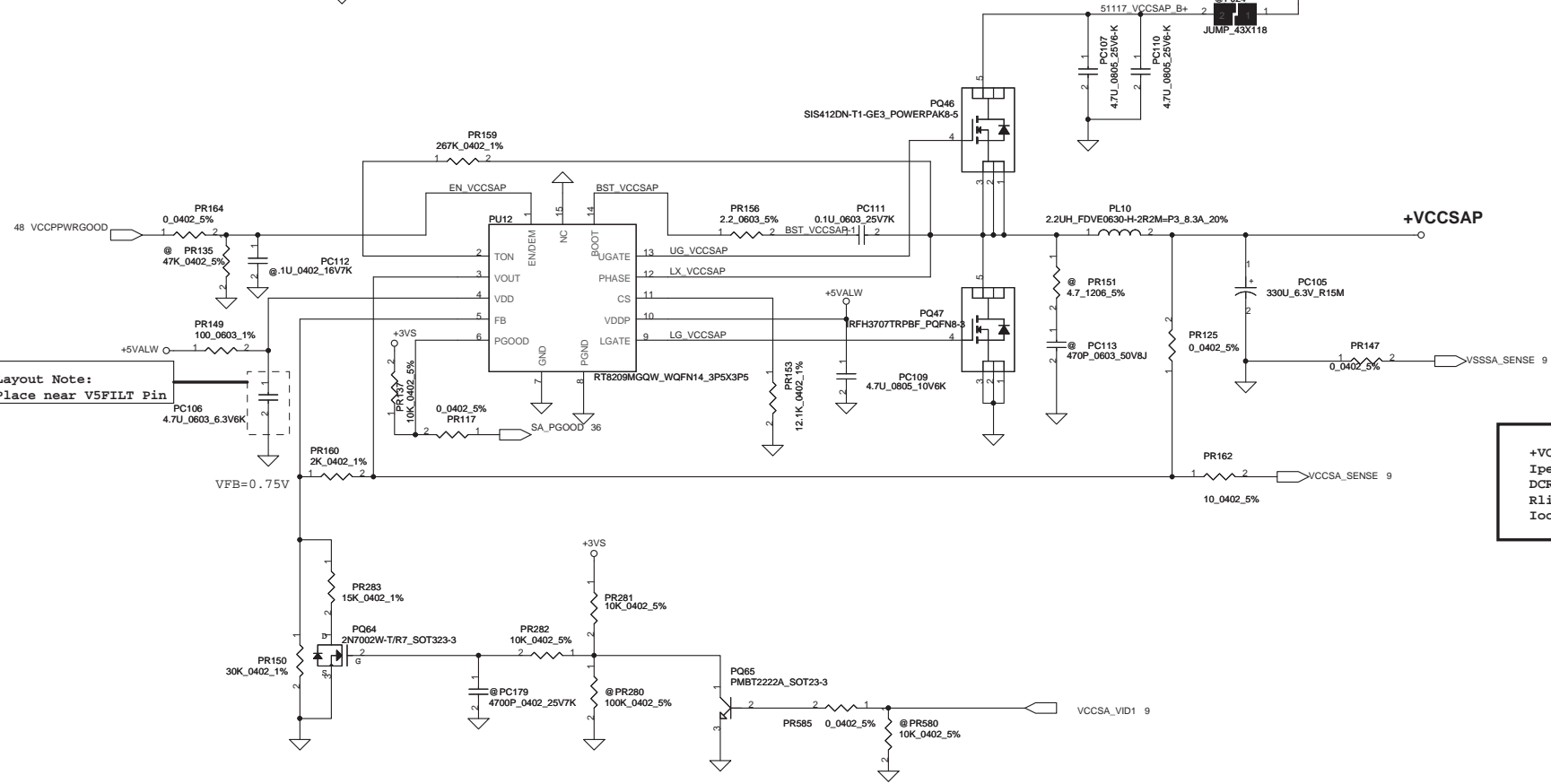
B+

+1.5VP  
Ipeak=21.56A;1.2Ipeak=25.87A ;Imax=15.09A  
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm  
Rtrip=16.5K  
Iocp=25.97A~42.41A

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1.8VSP  
 $I_{peak}=3.35A$  ;  $1.2I_{peak}=4.02$  ;  $I_{max}=2.345A$   
 $V_{out}=0.6*(1+(20K/10K))=1.8V$   
 -DVT-



+VCCSAP  
 $I_{peak}=6A$  ,  $I_{max}=4.2A$  ,  $1.2I_{peak}=7.2A$   
 $DCR= 9\text{ m}(\text{typ})-10\text{ m}(\text{max})$   
 $R_{limit}=12.1K, R_{dson}=14.5-17.9\text{ mohm}$   
 $I_{ocp}=7.24A-12.59A$

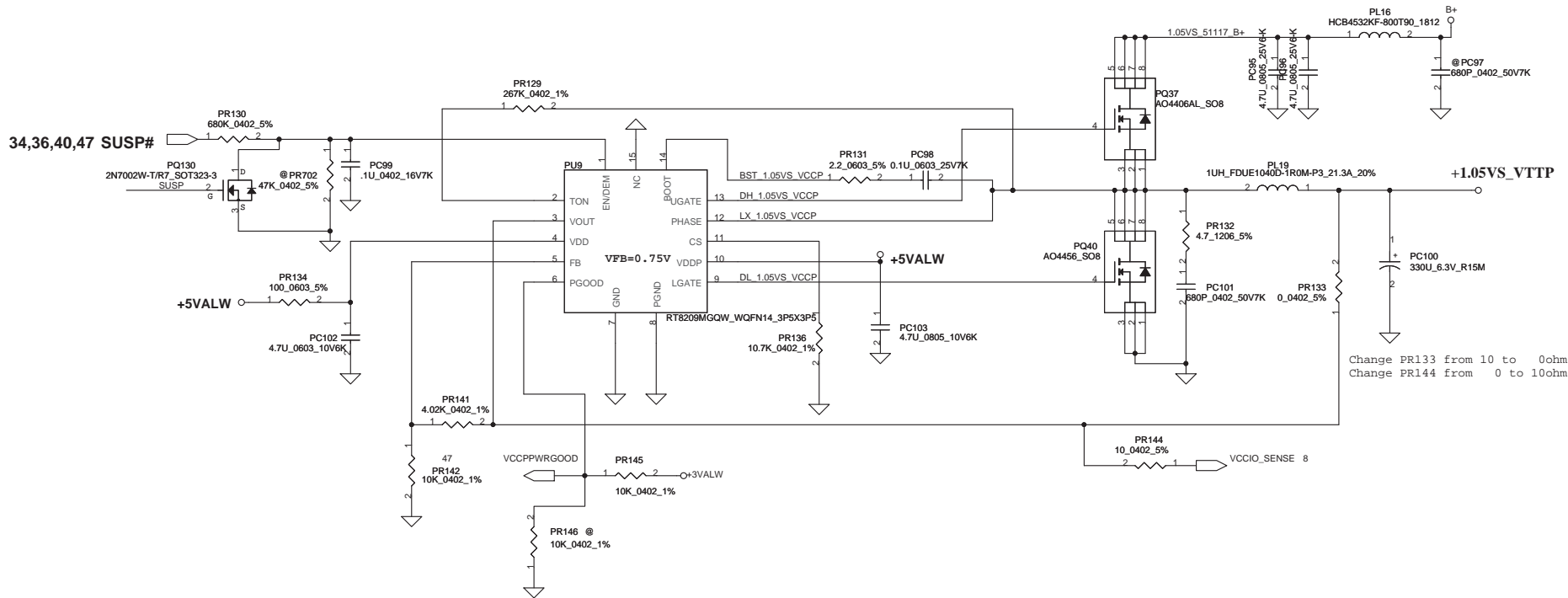
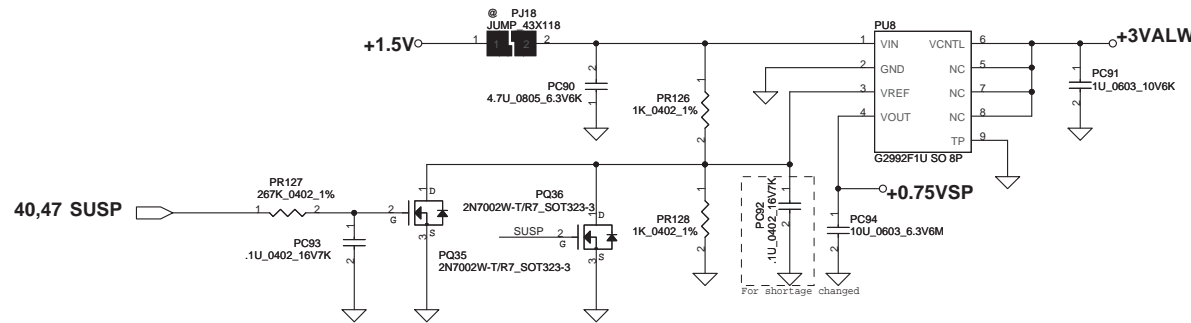
Layout Note:  
 Place near V5FILT Pin

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

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Note:Use VCCSA\_SEL to switch High & Low Level for VID[1]



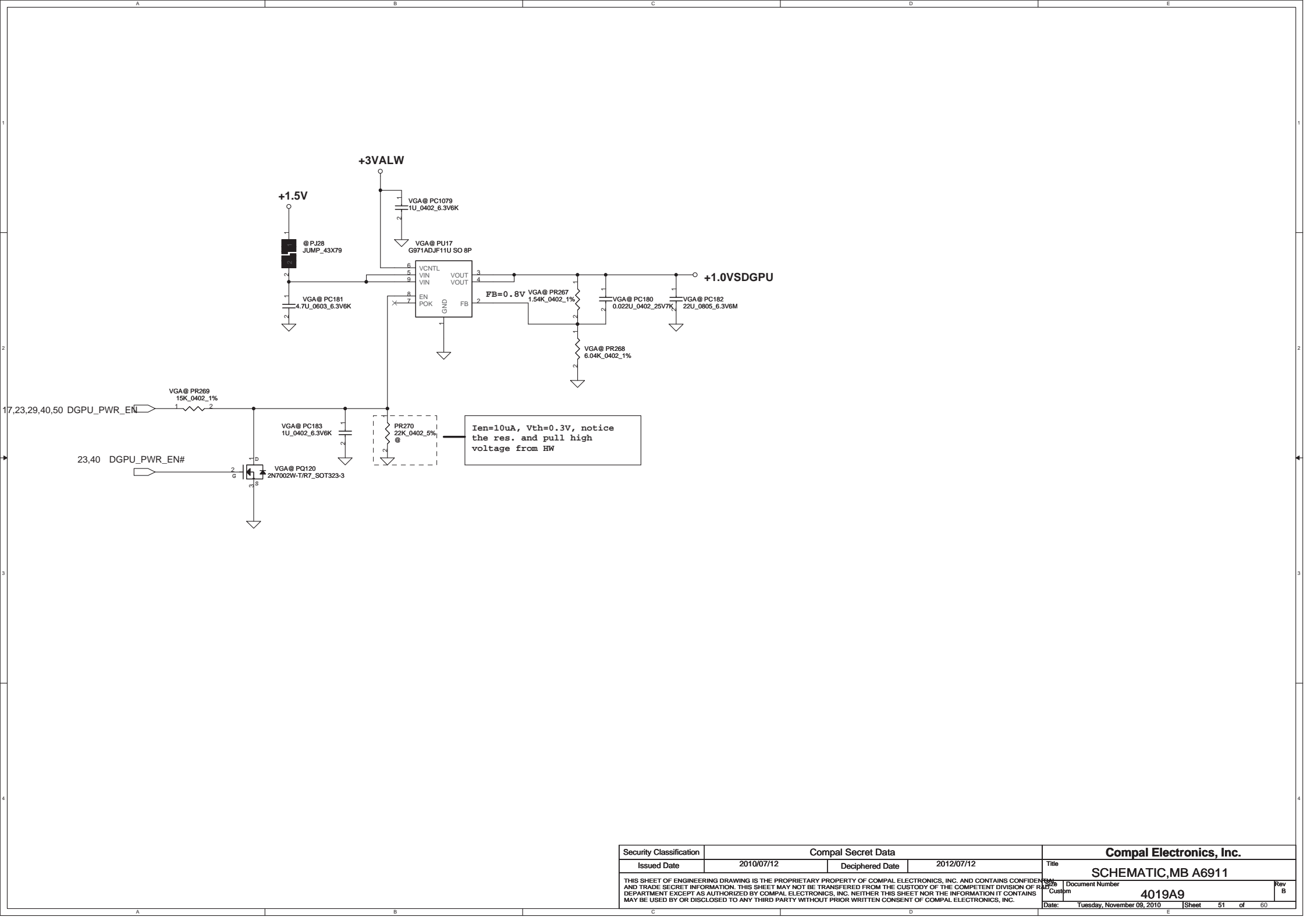


+1.05VS\_VTTP:  
 Ipeak=14.05A;Imax=9.84A;1.2Ipeak=16.86A  
 Rdson=4.5~5.6m ohm ; Freq=298KHz  
 Rtrip=10.7Kohm,Vtrip<200mV  
 Iocp=16.99A~27.73A

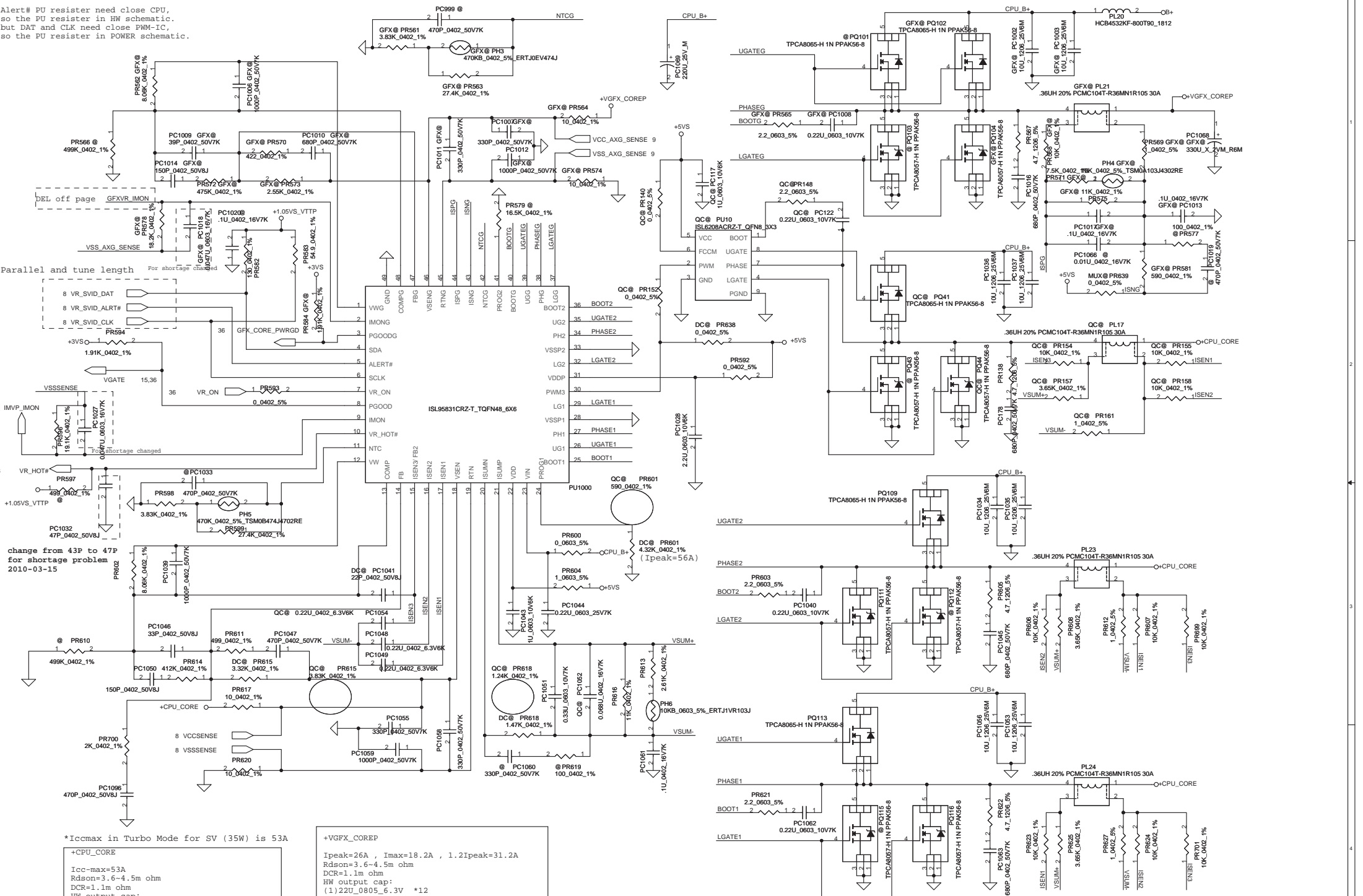
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Alert# PU resistor need close CPU,  
so the PU resistor in HW schematic.  
but DAT and CLK need close PWM-IC,  
so the PU resistor in POWER schematic.



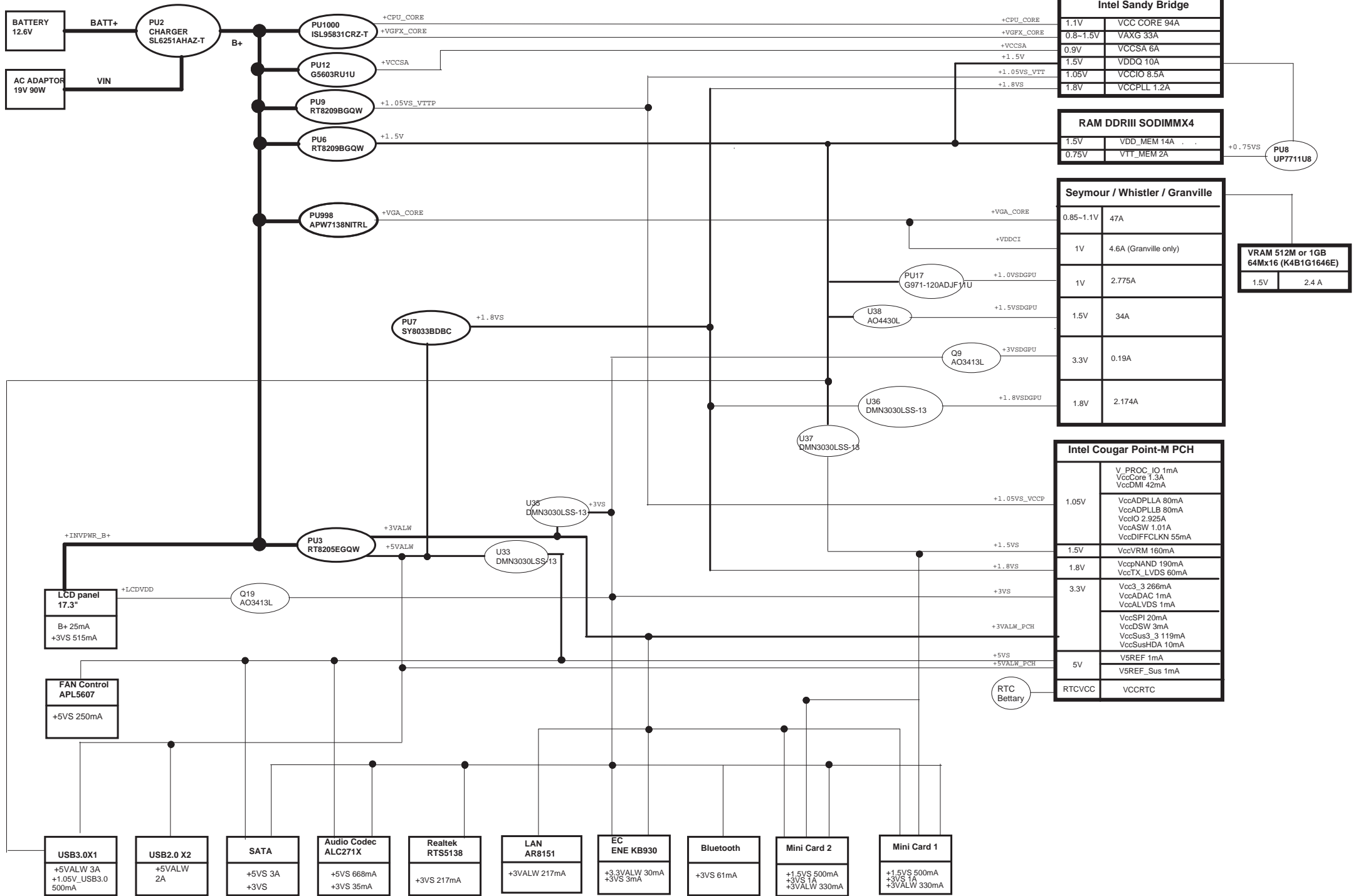
## Version change list (P.I.R. List)

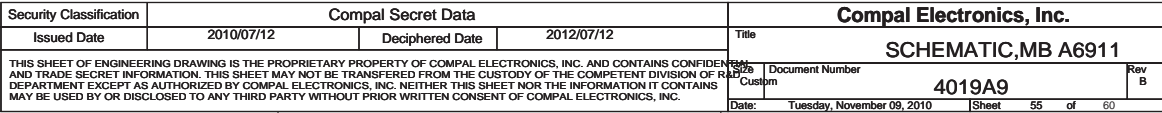
Page 1 of 1 for PWR

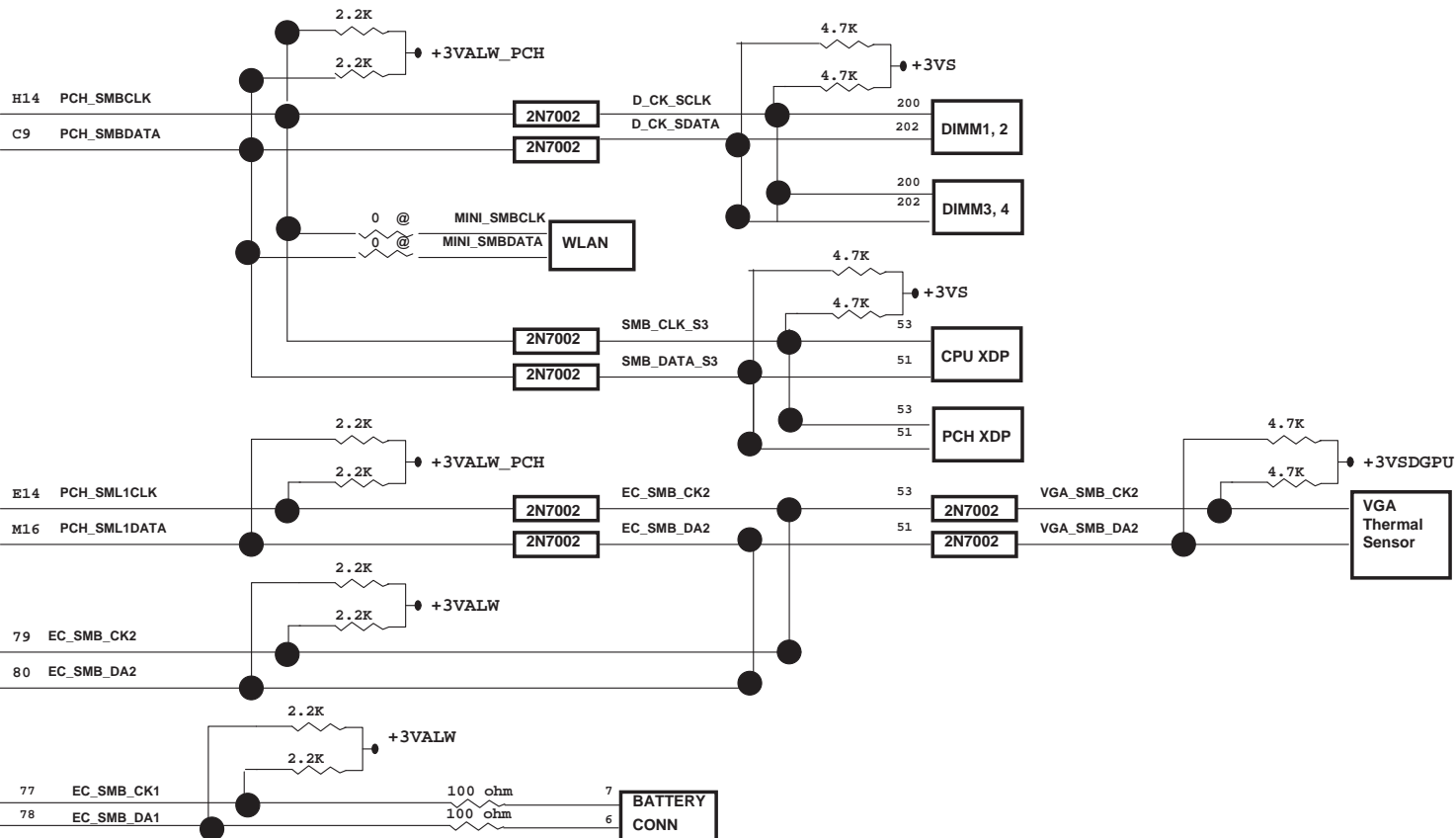
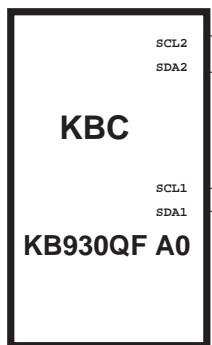
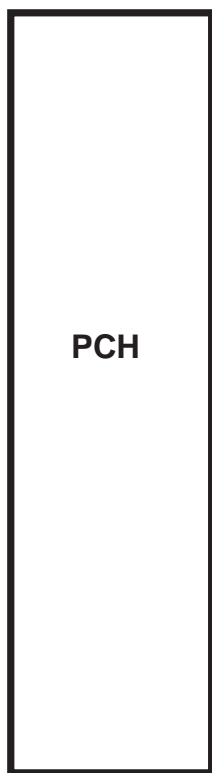
Item	Fixed Issue	Reason for change	Rev. PG#		Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002000.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Chnage PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放电.	HW request to add PQ130 and PQ131 to speed up to 放电.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargeable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 Change PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Chnage PL4 and PL5 to TOKO new part.	Chnage PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00. Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100b80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient reponds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% ADD PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Because original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Chnage PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Chnage PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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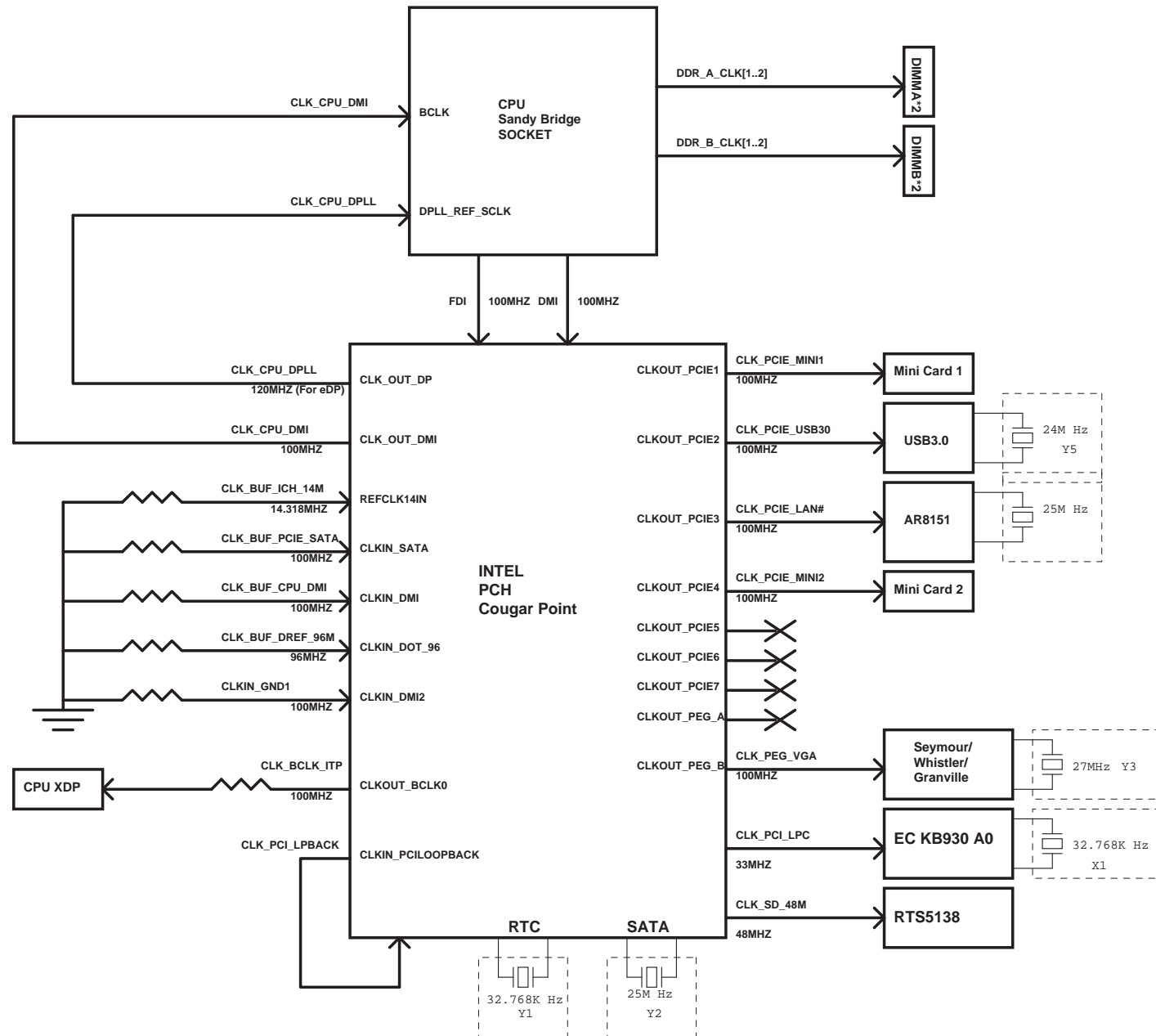




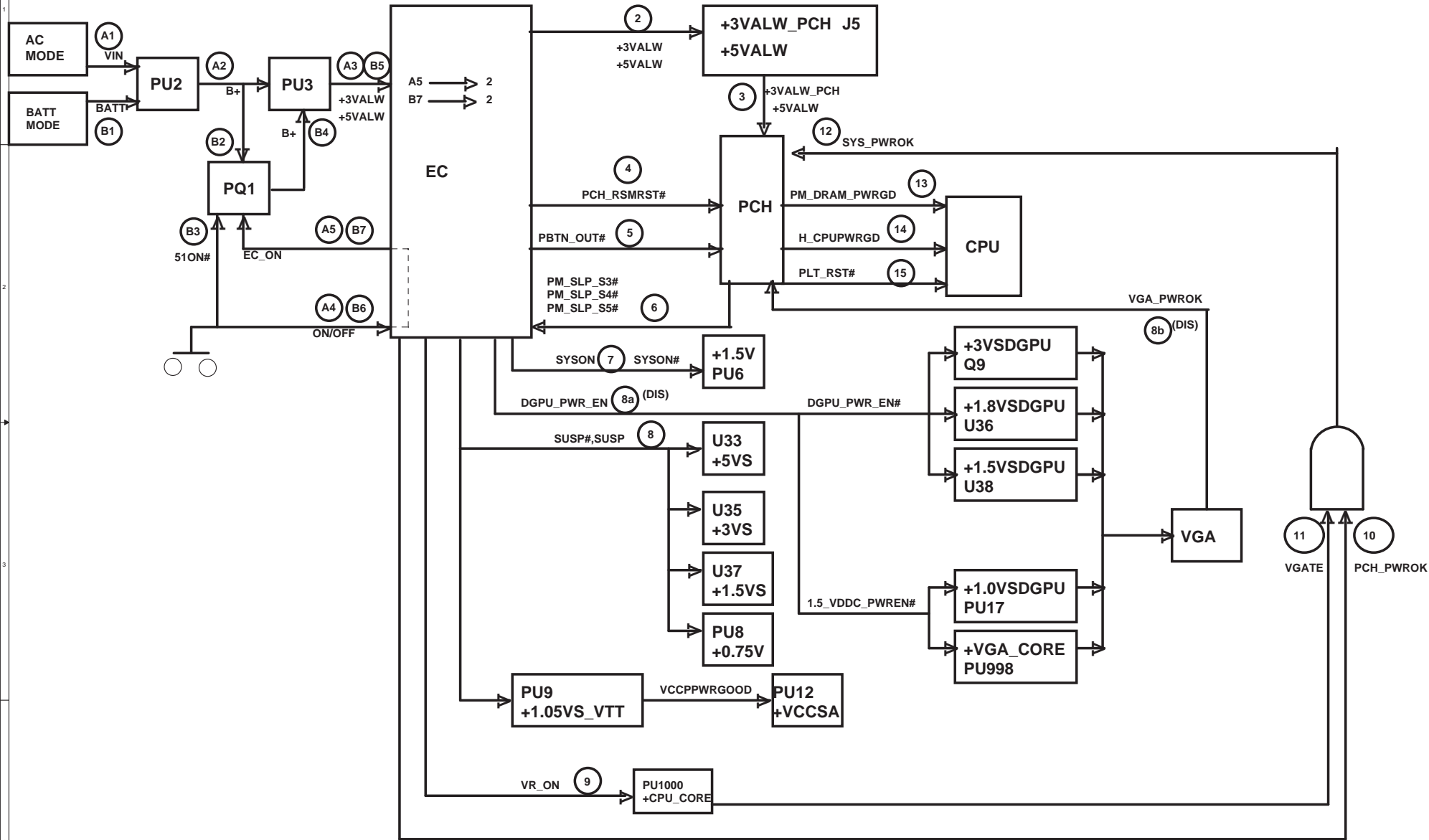
### PCH SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X
DIMM1 A2	1010 001X
ChannelB DIMM0 A4	1010 010X
DIMM1 A6	1010 011X

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PCB

LA-6911P MB Rev0: DA80000LC00  
LA-6911P MB Rev1: DA80000LC10  
LA-6911P MB with Small Board Rev1: DAZ  
LA-6911P REV0 MB

VGA

Granville PRO M2 A12:  
SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

WHISLER PRO M2 A11:  
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

X76

X761@ X76264BOL01 VRAM 512M SAM P7YE0  
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X762@ X76264BOL02 VRAM 512M HYN P7YE0  
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

X763@ X76264BOL03 VRAM 1G SAM P7YE0  
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X764@ X76264BOL04 VRAM 1G HYN P7YE0  
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

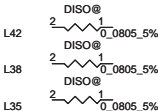
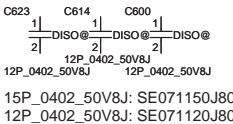
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X766@ X76264BOL06 VRAM 2G SAM P7YE0  
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

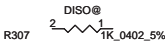
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Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X768@ X76264BOL08 VRAM 1G HYN P7YE0  
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

CRT Option Components

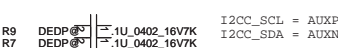
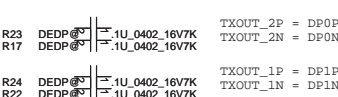


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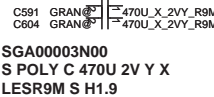


DIS only PCH DAC\_IREF  
can use 1K\_0402\_5% PD to GND

DIS EDP Option Components



Granville VGA\_CORE CAP Option



EC susclk/crystal  
Option Components





